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DEVELOPMENT OF FOCAL PLANE MULTIPLEXER

Science Center, Rockwell International
1049 Camino Dos Rios
Thousand Oaks, CA. 91360

February, 1977

FINAL TECHNICAL REPORT

1 February 1975 through 26 September 1976

Prepared for

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
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A hybrid focal plane technology which makes use of optimum detector and signal processor materials has been developed and successfully applied to the fabrication of a PbSnTe-silicon module, utilizing high performance backside-illuminated PbSnTe photodiode arrays. The thermal expansion mismatch between the two materials is accommodated by flexible metallic interconnects. Functional focal plane modules with devices on 4 mil centers in a 32x32 format have been fabricated and tested to temperatures as low as 4.2°K with charge storage operation of individual PbSnTe devices on the mated array at temperatures as

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high as 30°K. Arbitrarily long frame times are achieved with the FET switch array multiplexer used as a signal processor for this program. The structures fabricated withstand repeated thermal cycling to 4.2°K from room temperature while maintaining a high percentage of interconnections intact. The techniques developed during this program are more generally applicable to the fabrication of hybrid focal planes utilizing a wide variety of detector materials and signal processor configurations. Since the PbSnTe-Si structure successfully fabricated represents the single most difficult mechanical problem because of the large thermal expansion mismatch, all other direct mated detector-processor structures are, by comparison, very straightforward.

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DEVELOPMENT OF FOCAL PLANE MULTIPLEXER

J. M. Tracy and J. T. Longo

SAMSO TR NO. 77-6

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FINAL TECHNICAL REPORT

1 February 1975 through 26 September 1976

Science Center
Rockwell International

FOREWORD

This report was prepared by the Science Center, Rockwell International under contract F04701-75-C-0049. This report covers the period of 1 February 1975 through 26 September 1976, and is the Final Report on this contract. The work described herein was carried out by the Science Center, Rockwell International, Thousand Oaks, California.

The principal investigators were John Tracy and Joseph T. Longo. Additional project support was supplied by David Olsen and Mark Ewbank.

The program manager was Dr. A. S. Joseph. Technical consultation was supplied by A. Michael Andrews and Richard C. Eden.

This research was supported by the Advanced Research Projects Agency of the Department of Defense and was monitored by the United States Air Force, Hq. Space and Missile Systems Organization under the above contract.

ABSTRACT

A hybrid focal plane technology which makes use of optimum detector and signal processor materials has been developed and successfully applied to the fabrication of a PbSnTe-silicon module, utilizing high performance backside-illuminated PbSnTe photodiode arrays. The thermal expansion mismatch between the two materals is accommodated by flexible metallic interconnects. Functional focal plane modules with devices on 4 mil centers in a 32x32 format have been fabricated and tested to temperatures as low as 4.2°K with charge storage operation of individual PbSnTe devices on the mated array at temperatures as high as 30°K. Arbitrarily long frame times are achieved with the FET switch array multiplexer used as a signal processor for this program. The structures fabricated withstand repeated thermal cycling to 4.2°K from room temperature while maintaining a high percentage of interconnections intact. The techniques developed during this program are more generally applicable to the fabrication of hybrid focal planes utilizing a wide variety of detector materials and signal processor configurations. Since the PbSnTe-Si structure successfully fabricated represents the single most difficult mechanical problem because of the large thermal expansion mismatch, all other direct mated detector-processor structures are, by comparison, very straightforward.

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1.0 INTRODUCTION

This is the final report of contract No. F04701-75-C-0049. The purpose of this contract was to develop the techniques required to fabricate and test a two-dimensional multiplexed infrared focal plane for use in the 8 to 14μm spectral range. The focal plane consists of a high performance backside-illuminated PbSnTe photodiode mosaic physically mated to a silicon signal processor. This structure utilizes the optimum infrared detector material (PbSnTe) and the optimum signal processor material (silicon) mated together. In order to carry out the mating, methods were developed under this contract to fabricate a high density of metallic interconnects between the individual photodiode elements and the silicon signal processor.

For purposes of this effort, an FET switch array multiplexer was used as a signal processor. This choice was dictated by the need for a cost-effect demonstration device. The requirement that the photodiodes operate in internal charge storage mode was then a result of this decision to use an x-y addressed multiplexer. High performance diode array characteristics were achieved under a parallel contract.

As the discussion will show, the efforts toward an operational hybrid module were successful. Hybrid structures utilizing a high density of flexible metallic interconnects were constructed and successfully operated at low temperatures with the photodiodes operating in charge storage mode.

The techniques developed here are generally applicable to any silicon signal processor and any photodiode material. In an even broader sense, this program has formed a technology base useful for a large category of potential hybrid devices not previously feasible.

2.0 TECHNICAL APPROACH

2.1 Hybrid Structure Options

There are two basic approaches to the construction of a hybrid infrared focal plane which have been proposed in the past few years. Both approaches make use of a silicon signal processor to access individual photodiodes of an intrinsic detector array. This section discusses these two basic approaches and justifies the choice of a direct mated approach which has been developed under this contract.

2.1.1 Indirect Mating to Signal Processor

The term indirect mating is used to mean that the interconnections between individual intrinsic photodiodes and appropriate signal processor inputs is made through an intermediate material. In other words, the silicon signal processor chips are located remotely from the photodiode array. Interconnections on the photodiode array to the intermediate material are made in an optimum way and the interconnections from the intermediate material to the silicon signal processing chips are made in an optimum way also. This approach is schematically illustrated in Fig. 1. There are several advantages to this approach. First, the intermediate material can be expansion matched to the intrinsic photodiode material. This avoids the thermal expansion mismatch problem which dictates that the interconnections must be flexible, as will be discussed for the case of direct mating. Another advantage of indirect mating is that an arbitrarily large volume is available for the mounting of silicon signal processing chips. Since these chips are mounted remotely there is the possibility of separately heat sinking the chips and the photodiodes. Therefore, one is not constrained to utilize input circuits and multiplexers which have negligible dissipation and which must be fabricated into very small areas.

The overriding difficulty of the indirect mating approach is that the intermediate material which carries the interconnection between the photodiode and the signal processor must necessarily be a complicated three-dimensional structure to meet very tight geometrical tolerances.

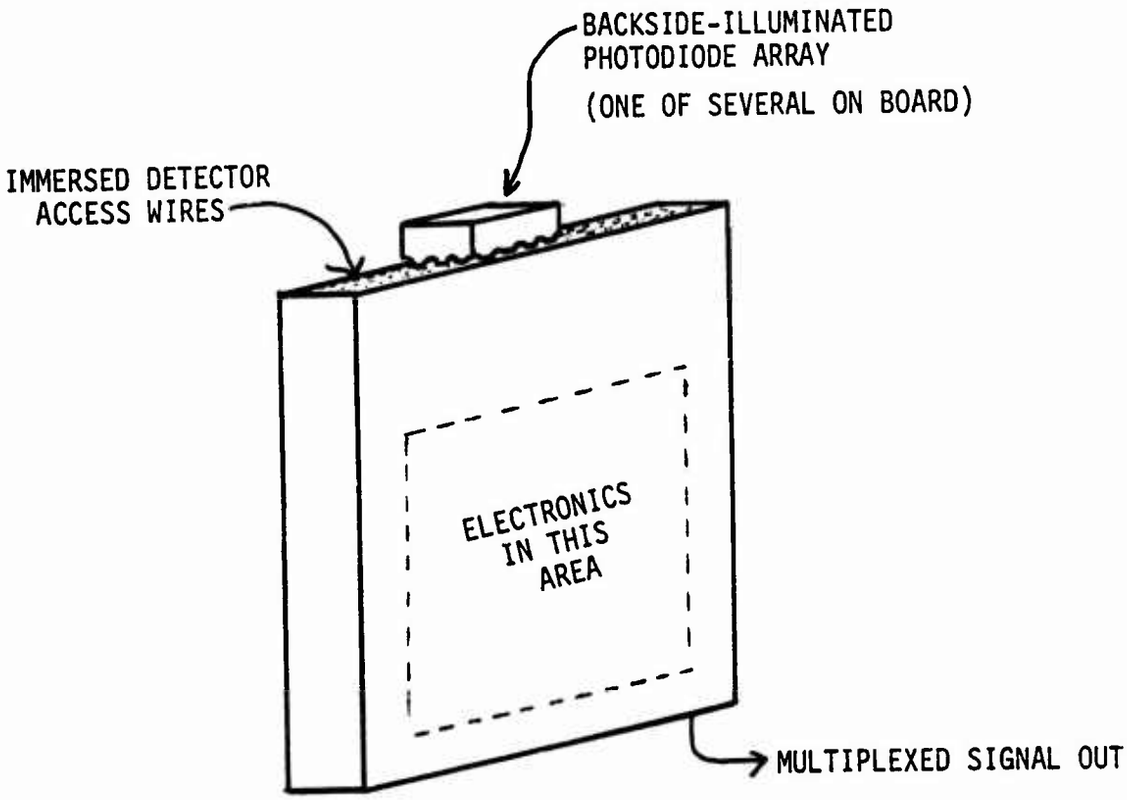


Fig. 1 Schematic representation of indirect mating approach.

Such a structure is not amenable to bulk planar processing and may therefore not be cost effective compared to the direct mated approach taken in this work.

2.1.2 Direct Mating to Signal Processor

The direct mating approach is shown schematically in Fig. 2. Here the intrinsic photodiode array is directly connected to the signal processing chip by means of a high density of short metallic interconnects. Assuming that the problems of thermal expansion mismatch and input circuitry can be solved, this structure offers the best choice for a cost effective hybrid infrared focal plane. Although the structure is three-dimensional the processing of the interconnects onto the silicon chip and the photodiodes on the intrinsic detector chip can be carried out by standard bulk processing techniques. In fact, it should be possible to fabricate all the interconnects needed for a complete wafer of silicon multiplexers during the same processing run in which the silicon circuitry is fabricated. The mating of the separately processed photodiode chip to the individual silicon die completes the focal planes module. Because of these advantages direct mating is seen as the most practical long term approach.

2.2 Physical Constraints on Direct Mated Hybrid

This section discusses the physical constraints which must be overcome in order to realize the structure shown in Fig. 2.

2.2.1 Backside Illumination

In order to realize the full potential of the three dimensional hybrid focal plane it is necessary that the structure have as large an optically active area as possible. If the photodiode array is to be realized as a single chip containing many photodiode elements, there are two modes of operation which must be considered as illustrated schematically in Fig. 3. Figure 3 (a) shows a structure in which the

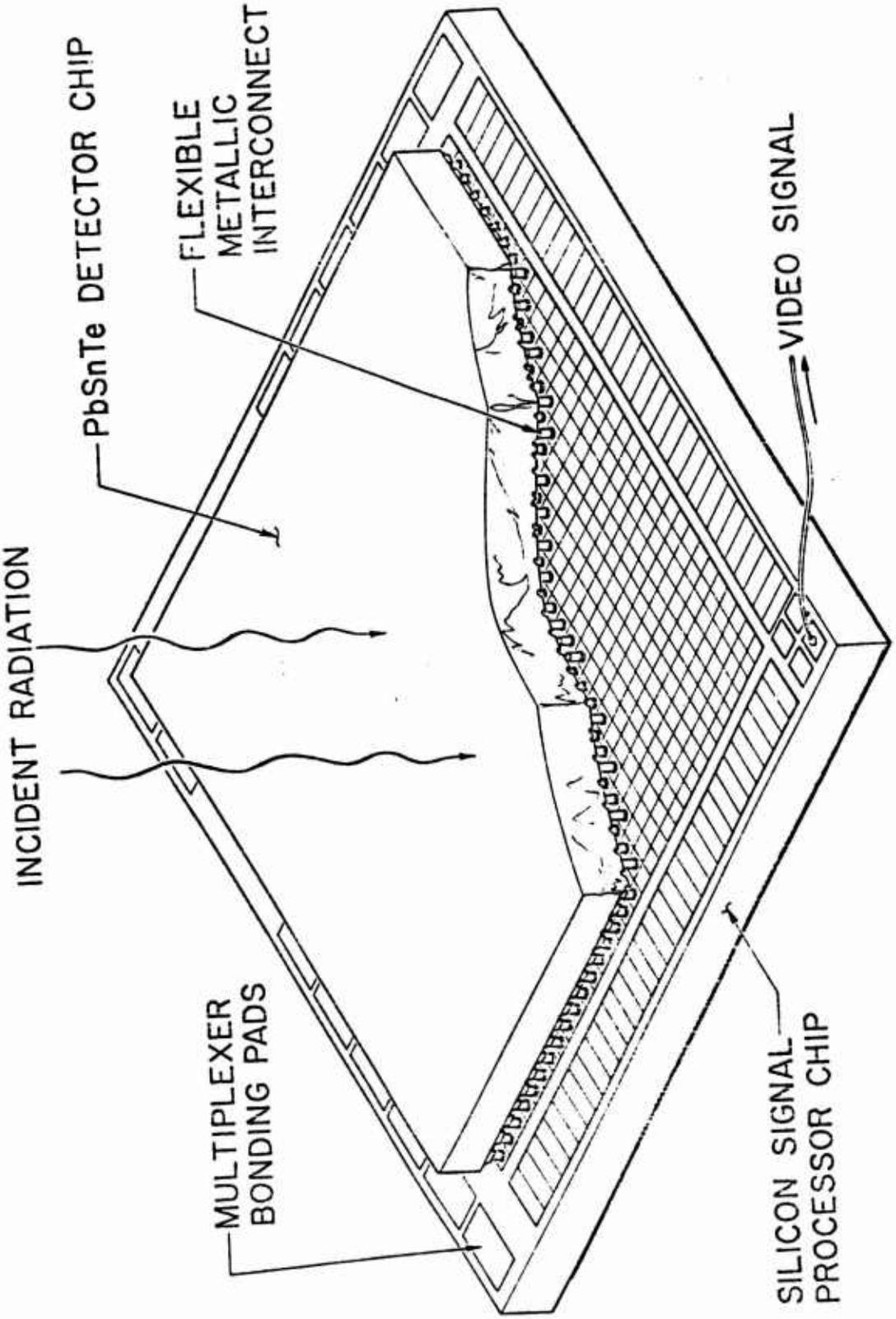


Fig. 2 Schematic representation of direct mating approach.

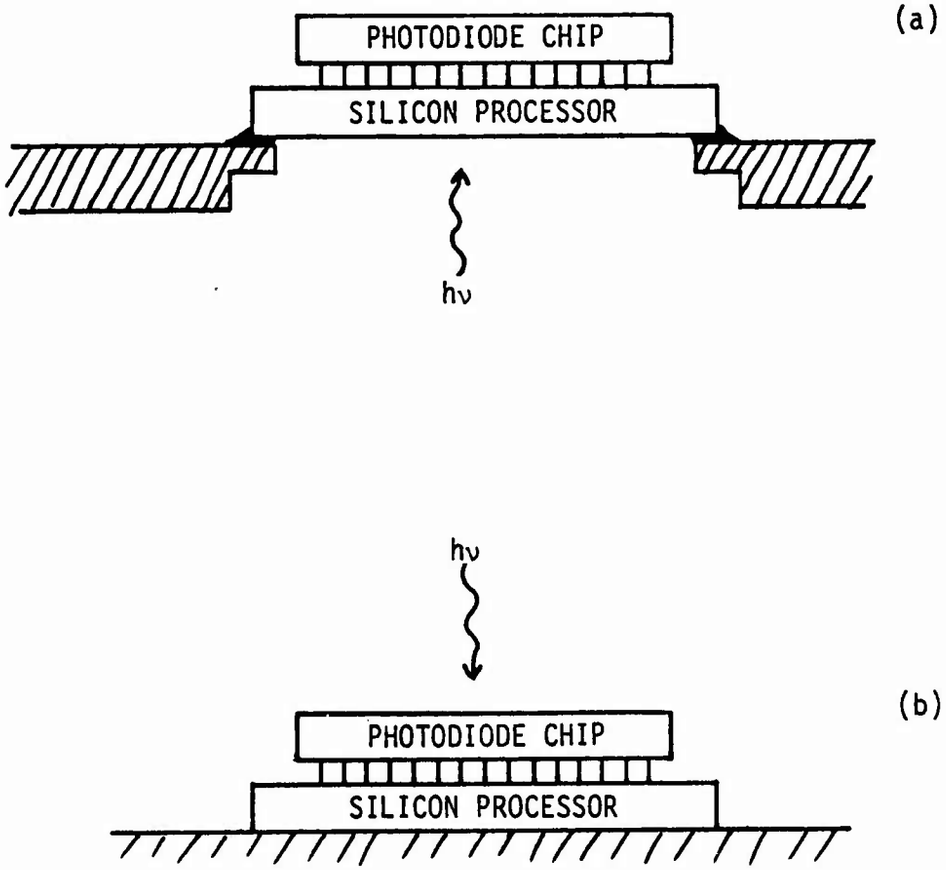


Fig. 3 Schematic drawing of alternative direct mated structures. (a) radiation enters through silicon signal processor. (b) radiation enters through photodiode substrate.

photodiodes are frontside-illuminated. In this arrangement the light enters the frontside of the photodiodes and the electrical signal is taken from the frontside. Because of this the light must enter through the silicon signal processor. Optically active area will be reduced for two reasons. First, opaque metal lines on the silicon wafer will obscure some of the light. Second, the metallic contact to the individual photodiodes will also result in a reduced optical efficiency. The arrangement shown in Fig. 3 (b) is preferred because the light enters through the backside or substrate of the photodiode chip. The frontside or mesa side of the individual photodiodes is available for metallization and there are no constraints on the construction of the silicon signal processor. It is this second structure to which this work is addressed.

The requirement for backside-illumination places additional constraints on the development of the photodiode material. The substrate must be transparent to the radiation in the wavelength region of interest. A successful program at the Science Center to develop high performance backside-illuminated diodes has made possible the realization of the hybrid structure shown in Fig. 3 (b). In this case the transparent substrate is PbTe. Photodiodes are constructed in an epitaxial layer of PbSnTe. Figure 4 shows a typical spectral response obtained with this backside-illuminated structure. One of the notable features of this type of spectral response is that no filter is required to suppress response to radiation below 6μm wavelength. External quantum efficiencies are in excess of 90%. Overall optically active area is approximately 70%; this value is enhanced by reflection from the curved valleys between mesas.

2.2.2 Charge Storage

The second constraint to be discussed is due to the fact that a two-dimensional array must be multiplexed. Since only one detector is being accessed at any given time the information representing the

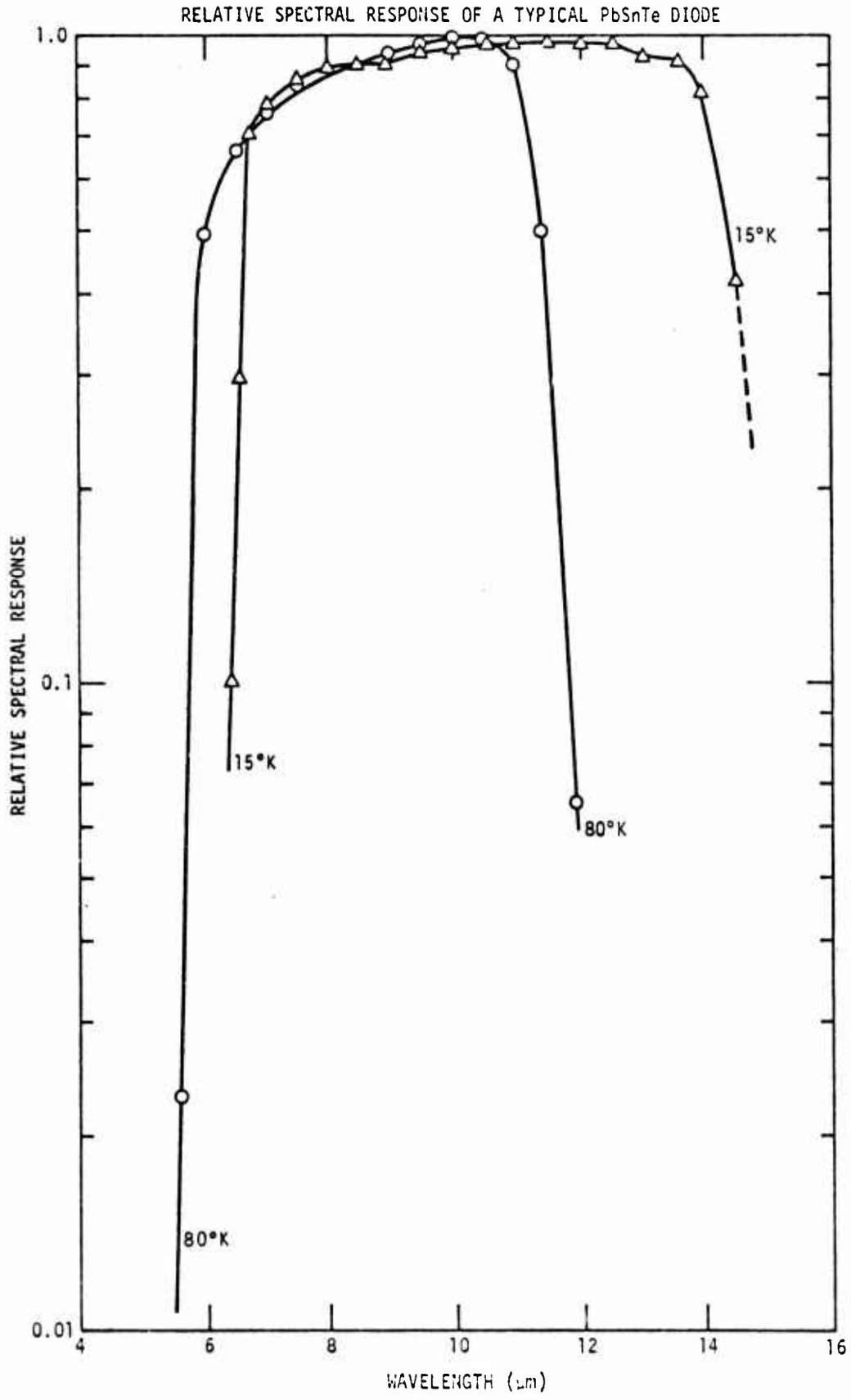


Fig. 4 Typical spectral response of backside-illuminated PbSnTe photodiodes at 80°K and 15°K.

accumulated photon flux on other detectors during the time in which they are not accessed must be stored in the vicinity of the photodiode and its input circuit. This information is stored in the form of electronic charges and may be accumulated either in the silicon signal processing circuitry or in the photodiode itself. For reasons which will be discussed later, the circuitry which would be needed to store the charge in the silicon processor chip was not available on the FET switch array multiplexers used for this development, therefore it was necessary to store charge in the photodidoes themselves. This was made possible by the development under contract No. F04701-74-C-0533 of high performance low leakage PbSnTe photodiodes whose leakage and capacitance characteristics made possible the accumulation of a large number of photo-generated charges. This was accomplished by initially reverse biasing the photodiodes and, during the time in which they were not directly accessed, allowing the incident photon flux to generate carriers which discharged the photodiodes. At the time of the next access the charge required to bring the photodiode back to the initial reverse bias was measured and taken to represent the number of photo-generated charges during the previous frame. The details of this type of operation are discussed more fully in Section 3.2.1 below. Although this mode of operation was necessitated by the use of a switch multiplexer, other types of silicon processing circuits in which the charge is accumulated in silicon storage wells would not require the device characteristics needed for the current development. This is because, for charge storage within photodiodes, an adequate reverse bias region of very low leakage must be provided. In the case of charge storage in the silicon wells it is only necessary to have adequately low leakage and adequately high device impedance in one biase-the operating bias.

2.2.3 Thermal Expansion Mismatch

One of the greatest difficulties which must be overcome is due to the thermal expansion mismatch between PbSnTe and silicon. Figure 5

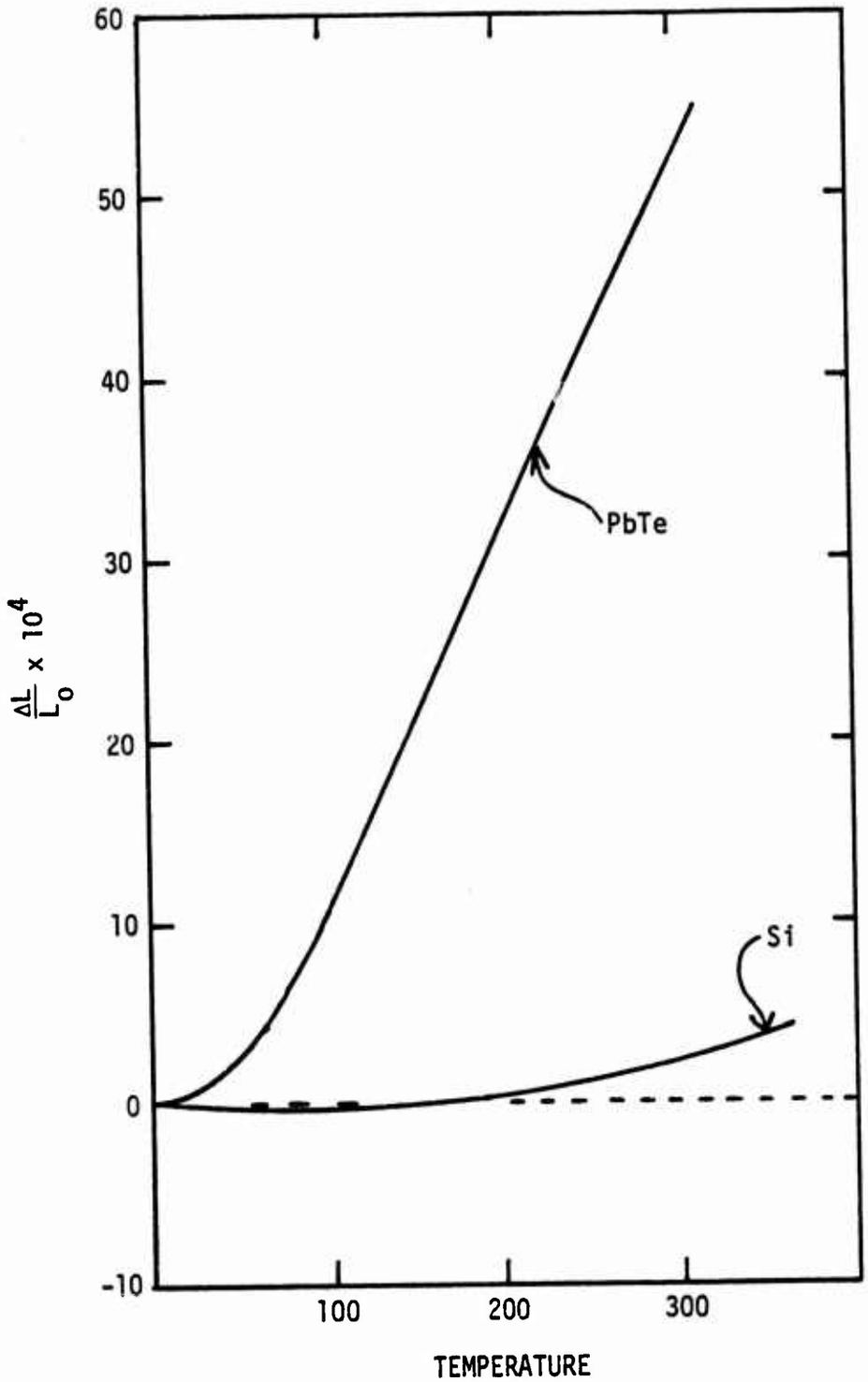
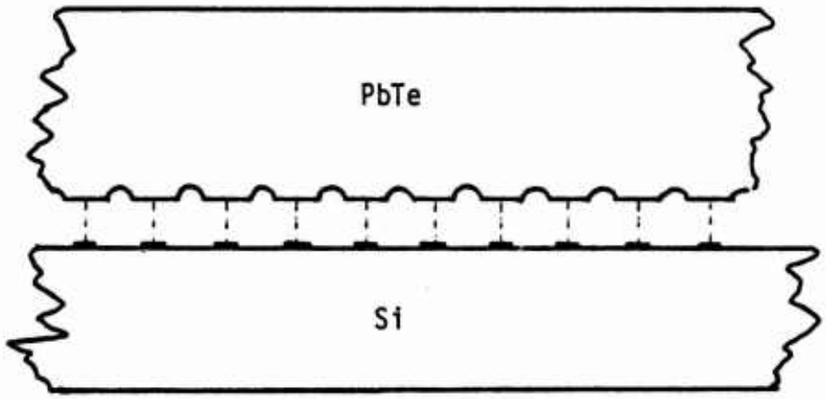


Fig. 5 Thermal expansion coefficients of PbTe and silicon versus temperature.

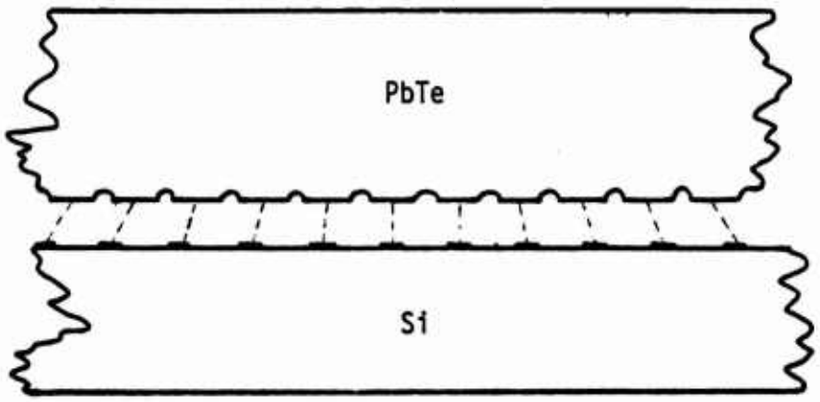
shows the thermal expansion coefficient for PbTe and for silicon. The PbTe coefficient is comparable to that of metals such as copper and aluminum while the silicon expansion coefficient is very small and in fact becomes slightly negative at lower temperatures. This means that on cooling to the operating temperature of approximately 30°K, photodiodes toward the outer edge of the structure will lose their registration with the corresponding input points on the silicon signal processor chip assuming that the structure is mated at room temperature. For a 32x32 element mosaic of devices on 4 mil centers, the loss of registration for the corner elements is substantial as is illustrated in Fig. 6. The corner PbSnTe elements actually move inward by approximately 1/2 mil for thermal cycling between room temperature and 30°K. Any rigid interconnection between the silicon and PbSnTe will result in tremendous strains in both the silicon and the PbSnTe material. In order to overcome this problem an approach in which the interconnects are made of a flexible or plastic material is desired. The interconnecting material must be able to move according to the schematic drawing in Fig. 6. The stresses required to deform the interconnecting material must be low enough so that damage does not occur in either the silicon or the photodiode material. In addition, the interconnecting material must have good electrical conductivity. These properties must be maintained from room temperature down to the operating temperature. The material chosen for this application is the metal indium. Indium was chosen because it fulfills all of the mechanical and electrical properties and interconnects in this material are easily fabricated. A complete discussion of the mechanical properties of indium interconnects is discussed in Section 3.4.2.

2.2.4 Power Dissipation

The final major constraint which had to be overcome was the power dissipation of the hybrid structure. Because the input circuitry is thermally so close to the operating photodiode any power dissipated



(a) At room temperature.



(b) At operating temperature.

Fig. 6 Schematic drawing of effects of thermal expansion on registration of detector elements after cooling to the operating temperature.

in this input circuitry will result in a temperature rise of the photodiode. Power dissipation in the photodiodes can be ignored because it is essentially that due to the radiation load from the incoming illumination. In low background applications this radiation load is low enough to be negligible. However, any source of heat in the vicinity of the metallic interconnect of the photodides will cause a substantial temperature rise because there is no heat flow path through the photodiode cells. Fortunately, the FET switch array multiplexer is an inherently low power device. The only sources of power dissipation in the required on-chip circuit reside in the shift registers. The present application required the design of a special shift register in order to operate the photodiodes at 30°K. This special shift register was successfully implemented and the total chip power dissipation reduced to negligible values. Careful analyses of the thermal situation will have to be carried out in any future application requiring the use of a different type of multiplexer chip such as a CCD.

2.3 Summary of Technical Approach

The technical approach taken in this development is summarized with the aid of Fig. 7. This figure shows a schematic cross section of the hybrid structure. Figures 2 and 7 can be compared to Figure 8 which shows a photograph of an actual operational hybrid focal plane made according to the approach discussed above.

The following is the work statement taken from the original proposal for this work. As the work progressed some modification to the tasks listed below were necessary. With these modifications incorporated into the task, the discussion which follows will show that all of the tasks have been accomplished in this development.

Task 1. Focal Plane Electronics

- Build a MOSFET recharge preamplifier.
- Modify existing clock circuits to give frame time up to 3 seconds and test dynamic shift registers for this capability.

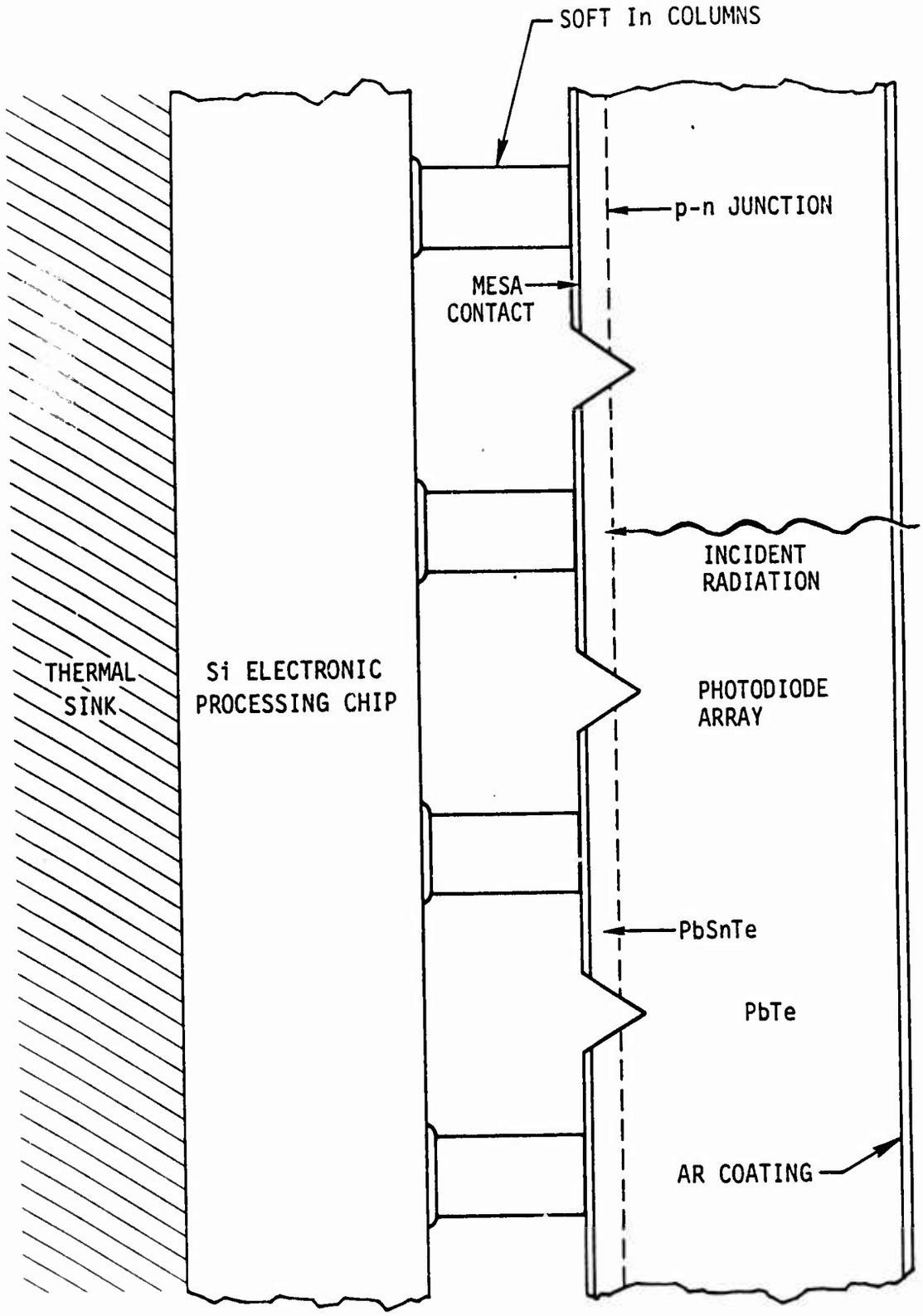


Fig. 7 Schematic drawing of hybrid structure cross-section showing flexible metallic interconnects.

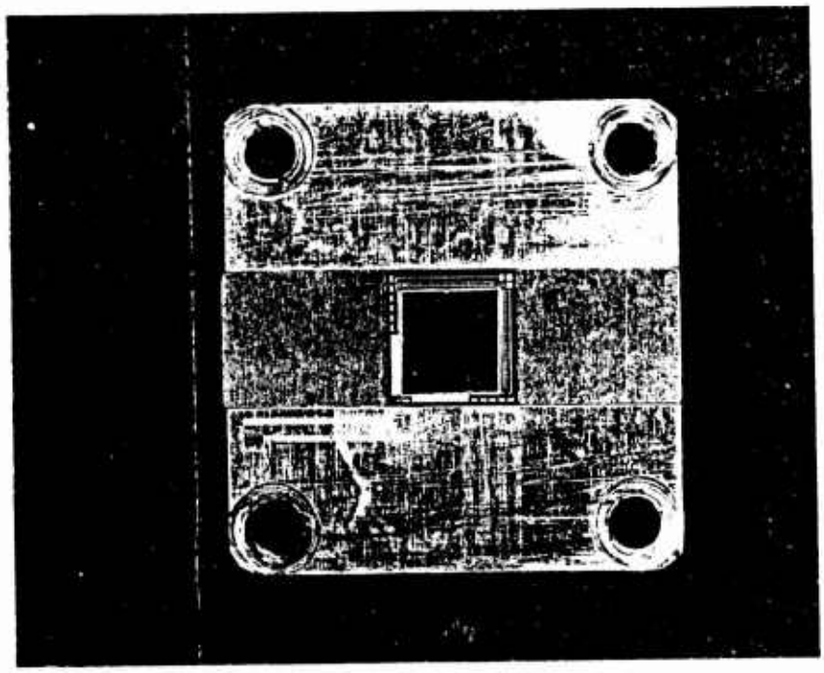


Fig. 8 Photograph of competed hybrid structure.

- Test the purchased Si chips for satisfactory operation at cryogenic temperatures.

Task 2. Wafer Mating

- Develop techniques for making indium contacts onto the silicon and PbSnTe contact pads.
- Develop techniques for mating and joining the wafers.

Task 3. Testing of Hybrid Array

- Develop techniques to use minicomputer for array tests.
- Test the completed array.
- Deliver one best-effort PbSnTe-Si hybrid array.

3.0 TECHNICAL DISCUSSION

This section contains a detailed discussion of the technical problems which formed the basis of this work. Several extended analyses are deferred to the Appendices.

3.1 PbSnTe Array Characteristics

The development of a high performance PbSnTe diode array has been carried out under a parallel contract. The device characteristics necessary for the fabrication of the high performance hybrid structure discussed in the last section are as follows:

Size: 4 mil x 4 mil

Leakage Current: $< 10^{-12}$ amp at 30 mV reverse-bias

Quantum Efficiency: > 90%

Optically Active Area: > 70%

Spectral Region: 8-14μm

Operating Temperature: 25°K or higher.

These characteristics applicable to individual devices have been achieved. In addition, certain requirements relative to the geometry of the mosaic array must be met. Aside from uniformity of characteristics and device size which are discussed in connection with the mosaic development it is necessary that the mosaic array have the proper geometry and that the individual photodiodes and photodiode grounds use the proper electrically conductive material for interconnection to the silicon signal processor. The interconnect contact fabrication is discussed in Section 3.4. Geometrial considerations are discussed in this section.

The requirement for well defined photodiode chip geometry is mandated in this development by the peripheral circuitry of the multiplexer signal processing circuit. It was found from experiments that the size of the photodiode array could be no larger than .136 inches on a side. Larger chips resulted in obscuration of bonding pads on the multiplexer dice. Chips smaller than .128 inches on a side would result in the loss of photodiode elements in the 32x32 arrays, therefore chip size selected was approximately .135 inches on a side. Beyond these considerations it was felt that future applications of this technology will require high density packing of photodiode chips such as has been discussed here. This requirement will mean that in addition to controlling the actual dimensions of the chip the size of the individual chip will need to be square and planar. That such gometry control can be accomplished is shown in Fig. 9. This shows a photograph of a corner of an array used for mating experiments. Note that the corner is square and that the sides are planar. These results were achieved by using a diamond saw to carry out the cutting. For this development individual chips were cut from a larger epitaxial layer. Mesas were fabricated after cutting. Additional effort expended toward the development of techniques for cutting after etching arrays from entire epitaxial layers may result in substantial time and therefore cost savings for future hybrid developments. However, for the small number of chips required for mating experiments in this program, the procedure of etching after cutting was quite satisfactory.

In addition to control of chip size and etch geometry it was necessary that both faces of the chip be very flat in order that uniform contact is made to the interconnections to the signal processor chip. Initial experiments showed that epitaxial layers grown on saw cut and etched PbSnTe substrates were not flat enough for mating of large area arrays. In many cases, twenty micrometer steps were found on chips intended for mating. This means that very much taller interconnects must be fabricated so that those corresponding to the higher photodiodes

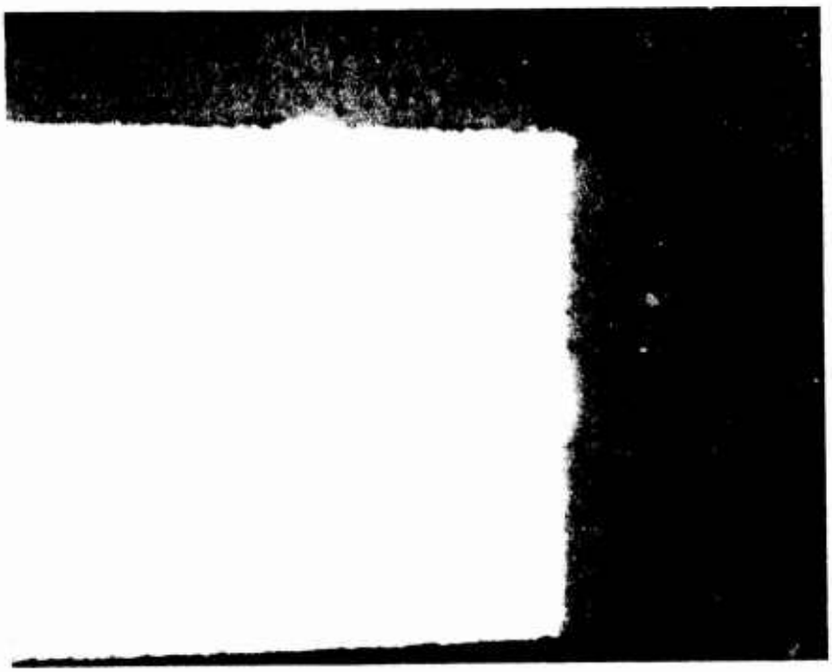


Fig. 9 Photograph of a corner of photodiode array showing geometry control. The distance from the corner to the valley is one mil.

could be adequately compressed so as to make contact. It was decided that the only way to overcome this difficulty was to polish the PbSnTe substrate material prior to epitaxial growth. Substrates were polished both on the epitaxial growth side and the side on which light would be incident because in the latter case it was necessary that flatness be achieved so that uniform mating pressure could be applied. If the incident light site of the substrate was not flat it was found that non-uniform pressure resulted in non-uniform interconnect contact and in some cases in fraturing of the photodiode chip. The results achieved by polishing the PbTe substrate is best illustrated with the help of Fig. 10. In this figure the DECTAK surface profile of a photodiode chip prior to mesa etching is shown. Both the epitaxial layer side and the substrate side are presented. It can be seen that the maximum variation across the chip of a size suitable for mating is less than one μm. This amount of non-uniformity is easily accommodated by plastic deformation of the indium interconnection.

3.2 Charge Storage Experiments

For resons discussed in Section 2.2.2 the individual PbSnTe photodiodes must, in this application, be operated in the internal charge storage mode. This mode of operation is common in wide bandgap photodiode structures. In fact, the multiplexer used in this program also incorporated a silicon photodiode operated in an internal charge storage mode. However, charge storage operation of a narrow bandgap diode has never previously been demonstrated. The first such demonstration was carried out during the course of this program. This section discusses those charge storage measurements as well as charge storage measurements carried out with the assistance of integrated FET switches contained in a custom linear multiplexer.

3.2.1 Charge Storage in Single Devices

Because internal charge storage is critical for the application under development in this program, an experiment was carried out early

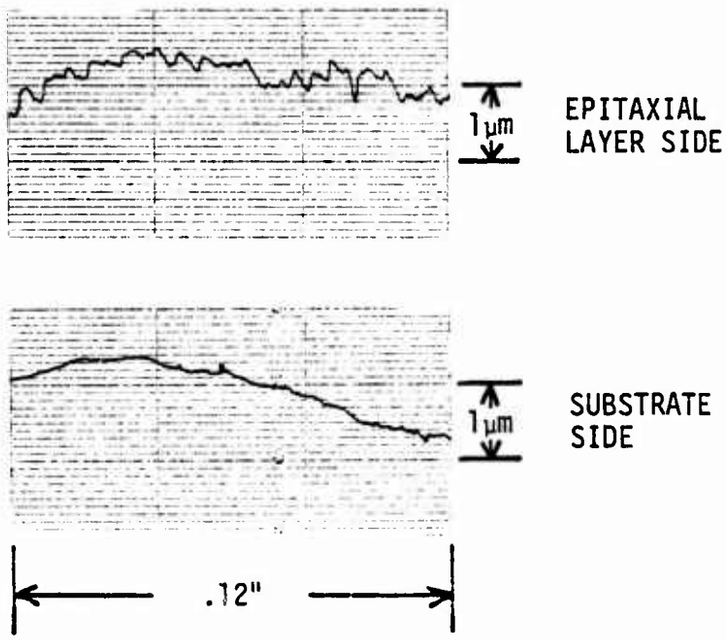


Fig. 10 Surface profile of photodiode chip. (a) substrate side. (b) epitaxial layer side.

in the program to demonstrate that the concept was feasible. This experiment made use of a single PbSnTe device in a cryogenic dewar connected to a single FET switch and a charge amplifier to simulate operation of a multiplexed detector operated in internal charge storage.

Figure 11 shows, in a schematic way, the principal of operation of a device operated in charge storage mode. When the switch is closed, the bias across the photodiode is just that of the battery voltage V_0. Upon opening the switch the device is no longer connected to the external source of bias and therefore the bias on the device will change with time according to the two sources of current flow. If there is no photon flux onto the device, only leakage current will discharge the photodiode. If photon flux is present, the rate of discharge will increase.

These ideas are best illustrated with the help of a simple diagram shown in Fig. 12. In order to construct these diagrams a very simple model is shown. In this model the capacitance and leakage current of the photodiode are taken to be bias voltage independent. In this case a plot of voltage across the diode versus time will be a straight line. Also, a plot of storage charge versus time will be a straight line. Both leakage and photocurrent tend to reduce the stored charge. If there is no device leakage then the reduction in the charge stored on the photodiode represents the integrated photocurrent since the device was last charged. By measuring the quantity of charge necessary to bring the bias on the detector back to its initial value the number of photo-generated charges can be obtained. By relating this to the device responsivity, the integrated number of photons impinging on the device during the preceding frame time can be calculated. When leakage is present, the situation is a little more complicated. Now the integrated number of charges lost due to leakage current must be taken into account in the calculation of the number of photo-generated charges. This can best be carried out by utilizing frame-to-frame subtraction. If the assumption

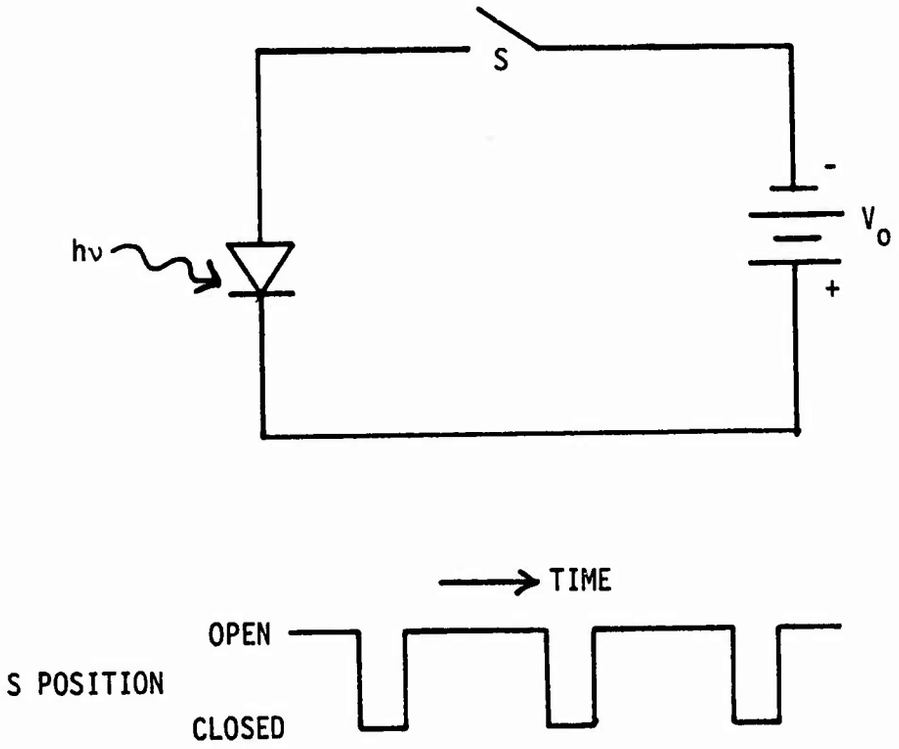
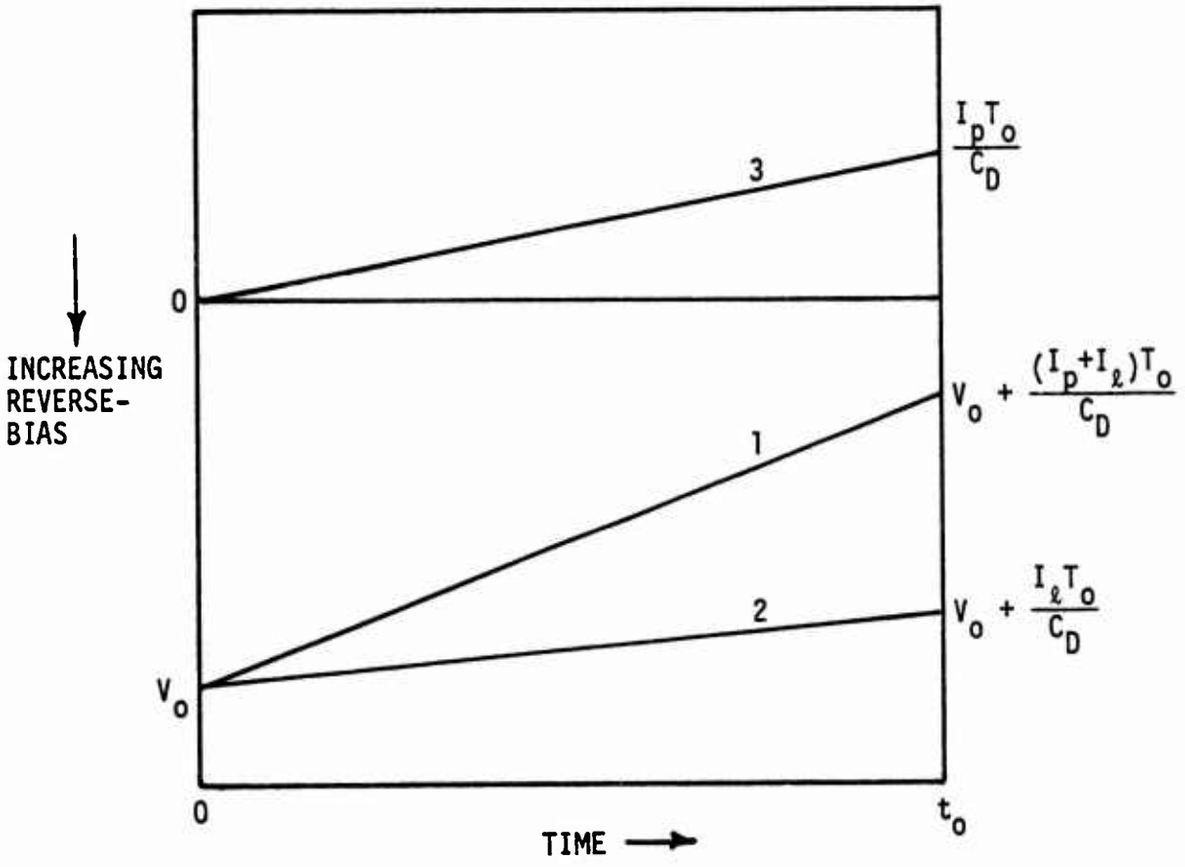


Fig. 11 Schematic drawing of principal of charge storage operation.



Curve 1: Photocurrent plus leakage present.

Curve 2: Leakage only present.

Curve 3: Due to photocurrent alone - obtained by subtracting Curve 2 from Curve 1.

Fig. 12 Diagrams showing time dependence of voltage across the photodiode for a device operating in charge storage mode. Diagram for stored charge would exhibit same time dependence.

is made that the leakage current is independent of the photon flux, then the number of charges lost due to leakage current can be determined during a frame in which there is no photon flux. Then an adjustment of the value obtained during an illuminated frame can be made by subtracting the charge necessary to recharge the device during the dark frame. Alternatively, the recharge signal from a given frame output can be subtracted from the previous frame. If this is done for each frame output the resulting differences represent the temporal changes in the illumination of a given photodiode element.

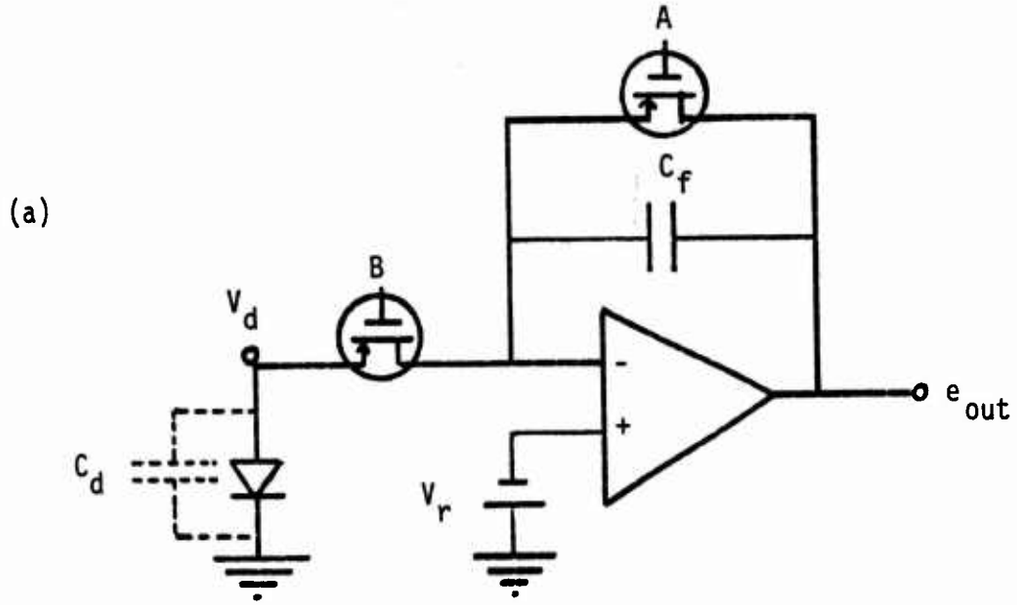
The actual situation is considerably more complicated than contained in the simple analysis above. This is because the actual device leakage current and capacitance are in fact dependent on the device bias. If leakage current is comparable to photocurrent, devices can still be used in charge storage operation, but the extraction of the photo-generated charge is more complex because the charge lost due to leakage current is itself dependent on the rate of decay of the detector bias and therefore on the photocurrent itself. Therefore the exact extraction of the photo-generated charge for the preceding frame-time involes the solution of an integral equation involving exact device parameters. Such conditions will occur if devices are operated at a high enough temperature so that device leakage is in fact comparable to photocurrent. However, if leakage characteristics are well behaved (that is nearly constant or linear with bias) and if the devices are operated at far enough reverse-biases so that the variation in capacitance is small, then a simple algorithm should serve to extract the signal.

Two methods could be used to detect the change in charge on the photodiode. One method would be to measure the bias remaining on the diode at the end of the frame time. Then, knowing the capacitance as a function of bias, one could calculate the lost charge. The second

method is to measure directly the charge needed to bring the bias back to the original point. Obviously this second method is preferred since it results in a measurement of the charge directly and at the same time recharges the device. Figure 13 (a) shows how this is implemented. The operational amplifier and its feedback capacitor form a charge integrator. When the FET switch is closed the bias on the device is brought to the same value as was applied to the non-inverting input of the amplifier (aside from a small offset voltage). Since the charge to change the detector bias is supplied from the output of the operational amplifier an equal amount of charge also is accumulated on the feedback capacitor. Therefore the change in the voltage across the feedback capacitor is a measure of the charge delivered to the photodiode. After each recharge it is necessary to reset the feedback capacitor. This is accomplished by a simple FET switch. After reset but before the next recharge the voltage at the output of the amplifier is just the bias voltage on the detector since the non-inverting and inverting terminals must be at that voltage.

The circuit just discussed was constructed from discrete components for the purpose for carrying out a charge storage experiment. A PbSnTe device was contained in a cryogenic dewar and held at a temperature of approximately 5°K. The recharge and reset switches were Texas Instruments 3N160 transistors. The amplifier used was a FET input operational amplifier. Clock waveforms for the switch gates and the idealized output waveform are shown in Fig. 13 (b). One aspect of this waveform which has not been discussed so far is the switching transients at every transition of the recharge and reset gate voltage. These transients, although large compared to changes in the signal voltage due to the actual signal, do not affect system performane if the timing of the gate waveforms is correct.

For now, the recharge signal is taken to be the difference in the output voltage just before and just after the recharge pulse.



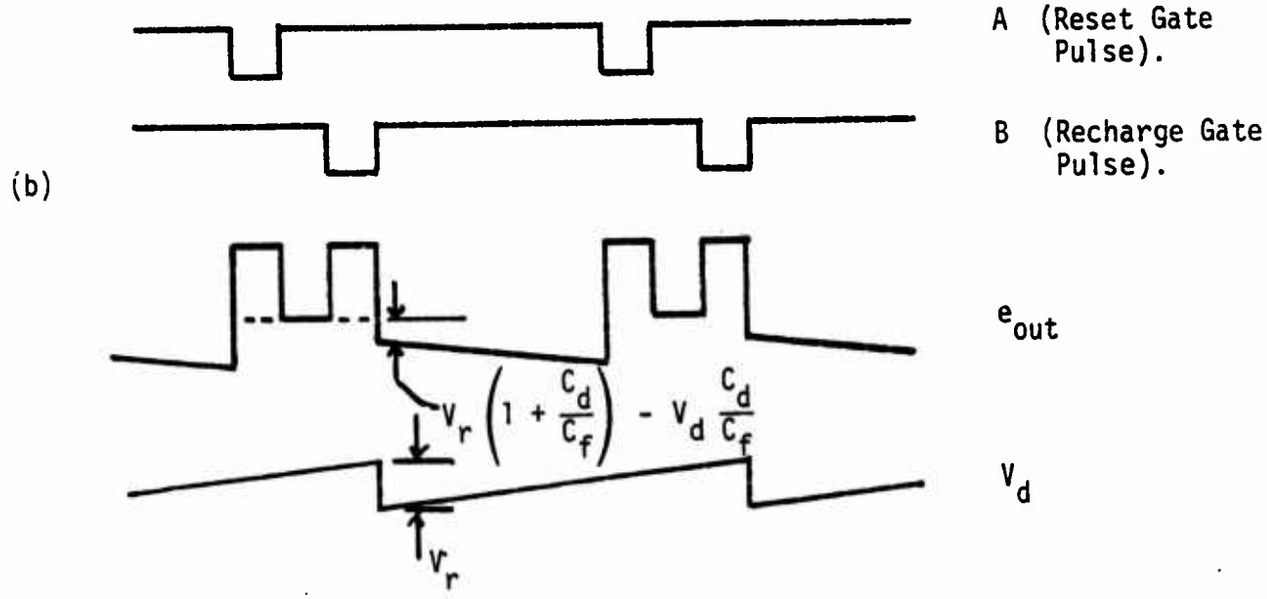
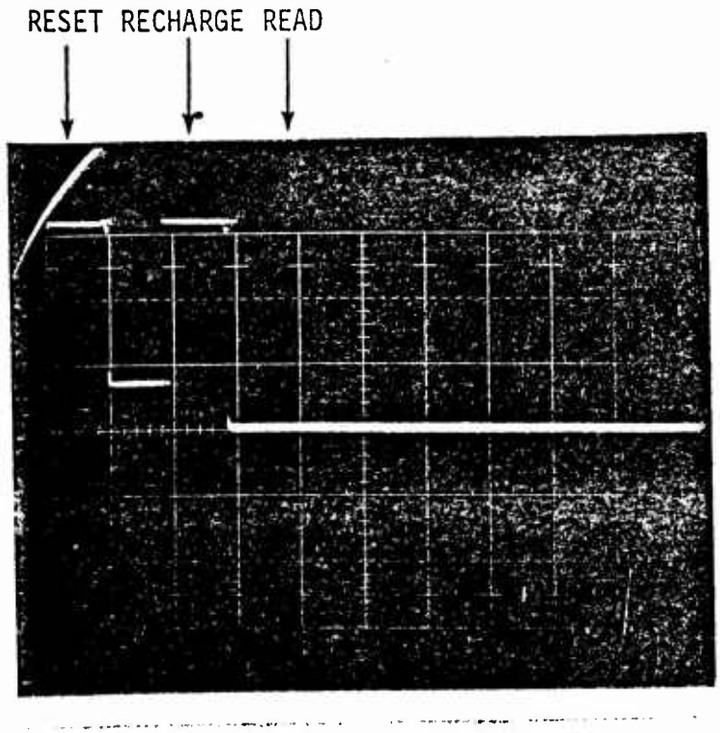
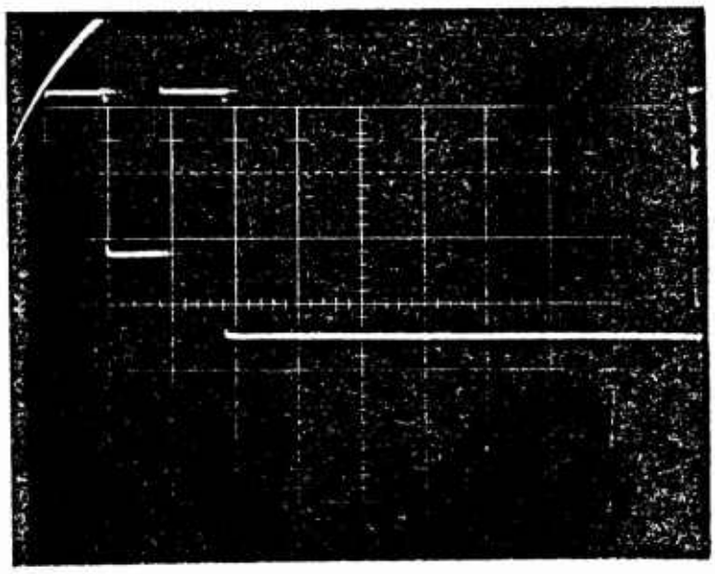


Fig. 13 (a) Schematic drawing of recharge amplifier circuit.
(b) Clock waveforms used to operate the circuit in (a).

The charge storage experiment was conducted by observing the output waveform on an oscilloscope. Error in reading the recharge signal voltage was approximately ± 1/2 millivolts. The recharge output was measured as a function of frame time and of detector photocurrent. Photocurrent was independently measured at zero-bias on a low noise amplifier. The most straight forward approach to verifying charge storage operation is to set V_r equal to a particular voltage and vary frame time and photocurrent to check for proper charge storage operation. The experiment was, in fact, carried out in this way. A simulator constructed with a silicon photodiode and a 100 picofarad capacitor was used as a check of proper system operation. Drawings of oscilloscope traces of the recharge amplifier output are shown in Fig. 14 for the case of no photocurrent and finite photocurrent. The rectangular parts of the waveform during reset and recharge are due to switching transients. Since the transient at the beginning and end of these time periods are equal in magnitude but opposite in sign, the integrated charge due to them is zero. The level during the read period has a slight ramp as shown in Fig. 13, but this is not observed in Fig. 14 because only a small part of the total frame time is shown. The ramp is due to operational amplifier current offset. This does not affect the results as long as the output is recorded at the beginning of the read time. For the traces shown, the frame time was 1.3 sec and the finite photocurrent was 7.5×10^{-13} amps corresponding to 5×10^{6} photons per second. Reading directly from the oscilloscope trace with no additional noise suppression, minimum detectable photoelectron flux was less than 10^{6} sec^{-1}. This noise level was limited by circuit interconnections and oscilloscope trace resolution rather than detector or recharge amplifier noise. Recharge occurs in less than a few microseconds and cannot be seen in the traces. Figure 15 contains plots of read voltage versus frame time for several different photocurrents. In this figure, V_r is set at -30 mV. Similar results for V_r = -75 mV are shown in Fig. 16. The read voltage



(a) DARK



(b) PHOTOCURRENT = 7.5×10^{-13} AMPS,
$N \approx 5 \times 10^{6}$ PHOTONS/SEC.

Fig. 14 Output voltage waveform for the single device charge storage experiments.

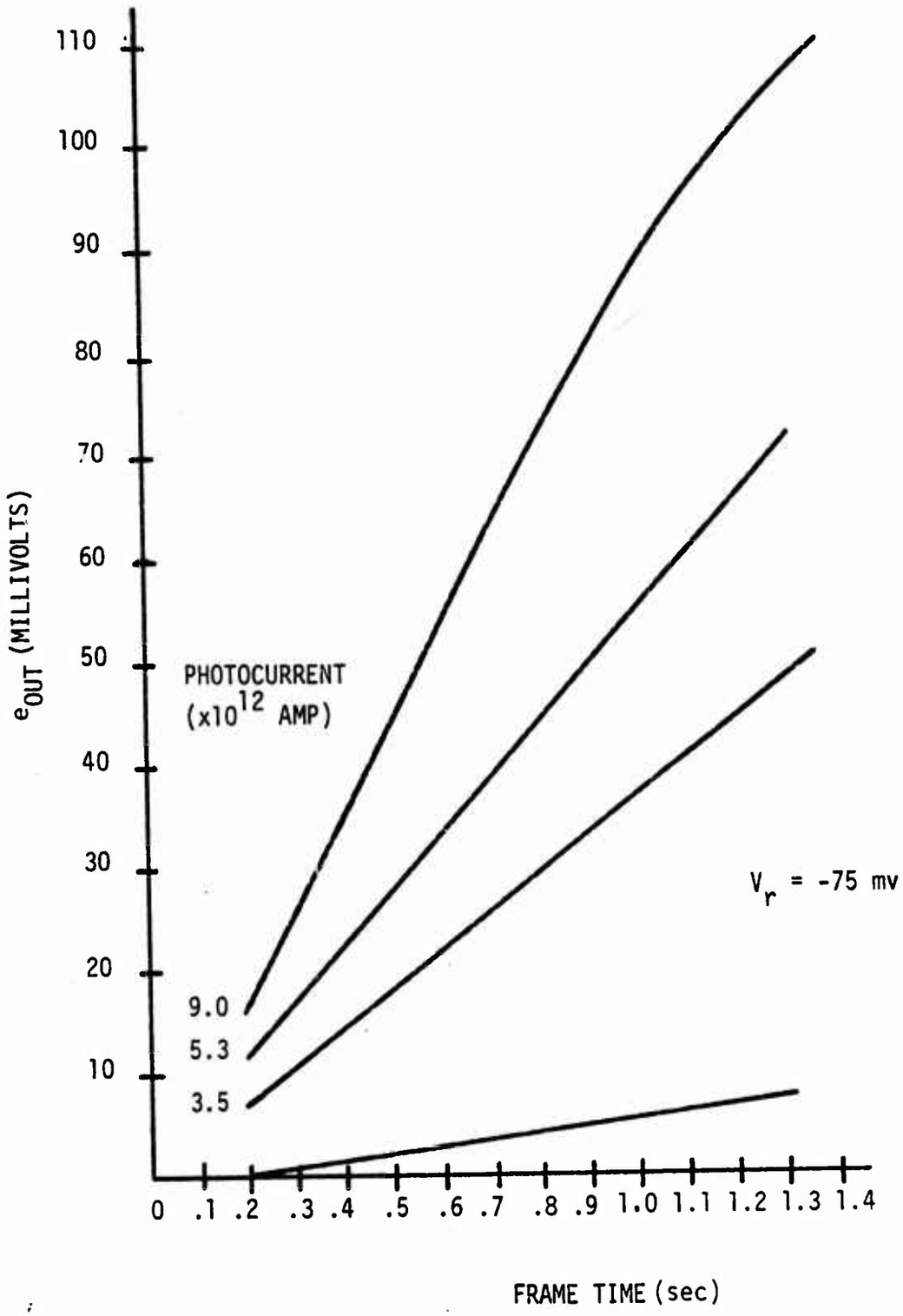


Fig. 15 Output voltage versus frame time for charge storage experiments. V_r = 30 mV.

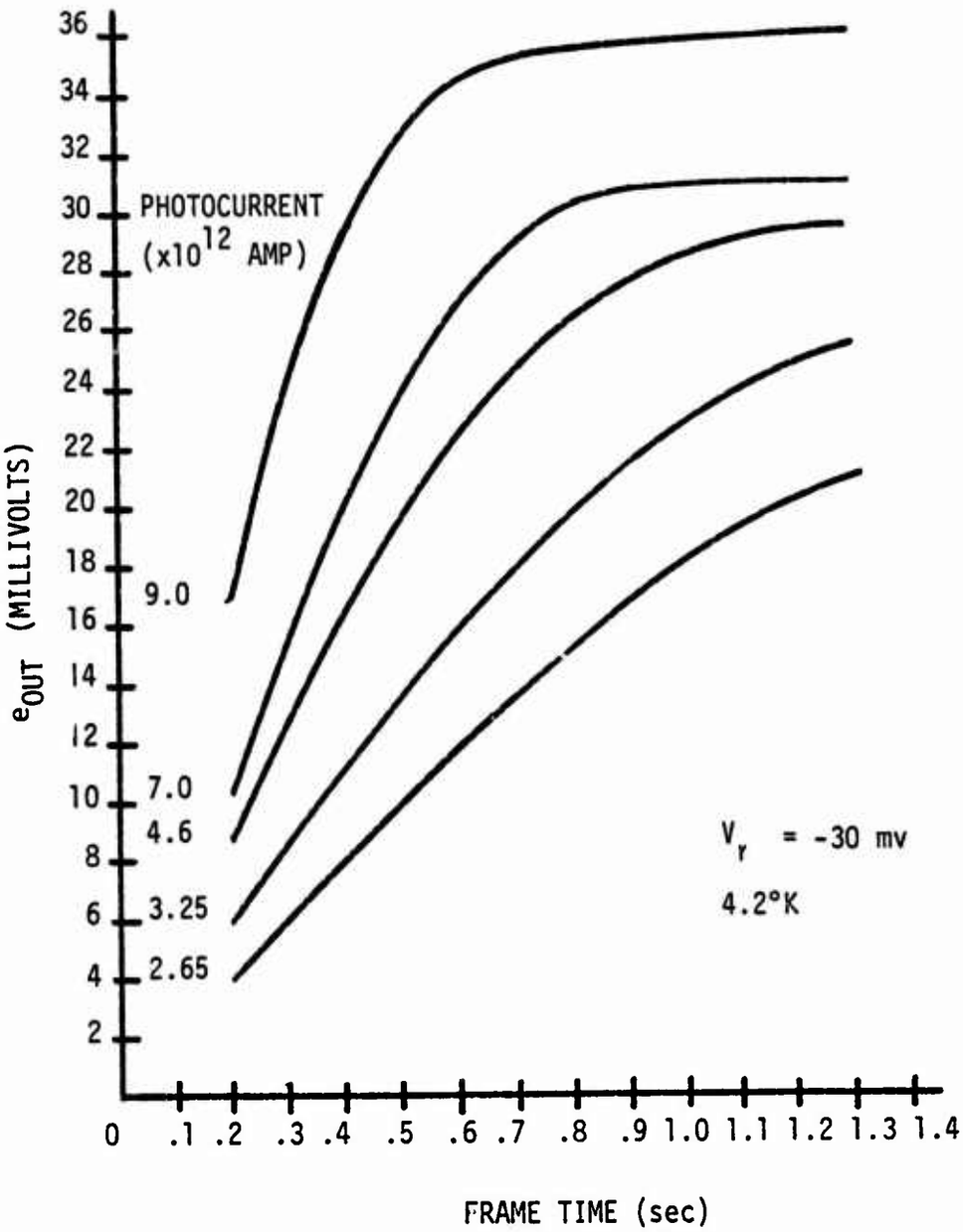


Fig. 16 Output voltage versus frame time for charge storage experiments. V_r = -75 mV.

given here actually has V_r subtracted out since the output is offset by this amount. At first glance, we can see that these curves have the expected behavior for charge storage operation. A nearly linear behavior is seen at short frame times and at low photocurrents. Saturation occurs at large accumulated photocurrent when the devices are fully discharged and become forward-biased. Saturation level is different for different photocurrent values because the devices go into forward-bias until forward conduction equals photocurrent and charge can no longer accumulate.

Some additional observations can be made. In the simple model above where it was first assumed that leakage current and capacitance were voltage independent, the variation of output voltage with frame time should be a straight line. It can be seen that, in fact, the variations of the recharge output are very accurately described by straight lines at the lower photocurrents. However, for the lower bias value, -30 mV, the plots at shorter frame time do have some curvature. This reflects the fact that the capacitance changes much more abruptly near zero bias and for a smaller absolute value of V_r discharge of the device into a region of lower bias occurs at shorter frame times for a given photocurrent.

This experiment shows unambiguously that the concept of charge storage in narrow-gap semiconnectors is feasible.

3.2.2 Electrical Mating to Linear Multiplexer

The experimental arrangement discussed in the last section was the simplest possible to demonstrate the concept of charge storage. However, that circuit utilized discrete devices for the recharge switches. The next major step was to demonstrate that recharge operation could be obtained using switches constructed in the same manner as would be required for the final multiplexer. This was accomplished with the aid of a custom linear multiplexer obtained from Reticon Corporation. This 64 element linear multiplexer contained FET switches identical to those

which would be found on a 32x32 element multiplexer to be obtained later. Access to the sources of the FET switches was available by means of special metal pads. Therefore, it was possible to wire bond directly between the source of the switch and a PbSnTe device. Further details of the linear multiplexer are contained in the next section of this report. For the purposes of the present discussion, this device served to provide the recharge switch previously found in the room temperature apparatus in the experiment just discussed.

Figure 17 is a drawing of the cold end of the apparatus used for the electrical mating experiments with the linear multiplexer. The specially designed header allowed incident infrared radiation to impinge on the PbSnTe detectors while maintaining the multiplexer circuitry in a shielded cold container. The temperature of the device was measured directly on the header using gallium arsenide diode thermometer. On the header, the silicon chip substrate is isolated from ground and maintained at ± 5 V. Electrical connection is made by bonding directly from the multiplexer pads to the PbSnTe. The PbSnTe bond is made using the thermocompression bonder. Then the wire is brought to the multiplexer ;ad and a stich bond is made. This later bond is very difficult to make because the pads are only 1.5 mil wide. Clocking of the linear multiplexer is carried out in such a way that the recharge and reset waveforms were as shown in Fig. 13. Measurements were made by reading the recharge pulse level on an oscilloscope with the vertical scale expanded so the pulse level could be read to the accuracy permitted by the system noise. Figure 18 is a photograph of the oscilloscope trace. The sloping line shows the position of a leaky device while the square pulses are devices operating in charge storage. On this particular array five devices were bonded to separate pads on the multiplexer.

The experimental apparatus was arranged so that PbSnTe devices could be exposed alternately to a 300°K or 650°K background. A small

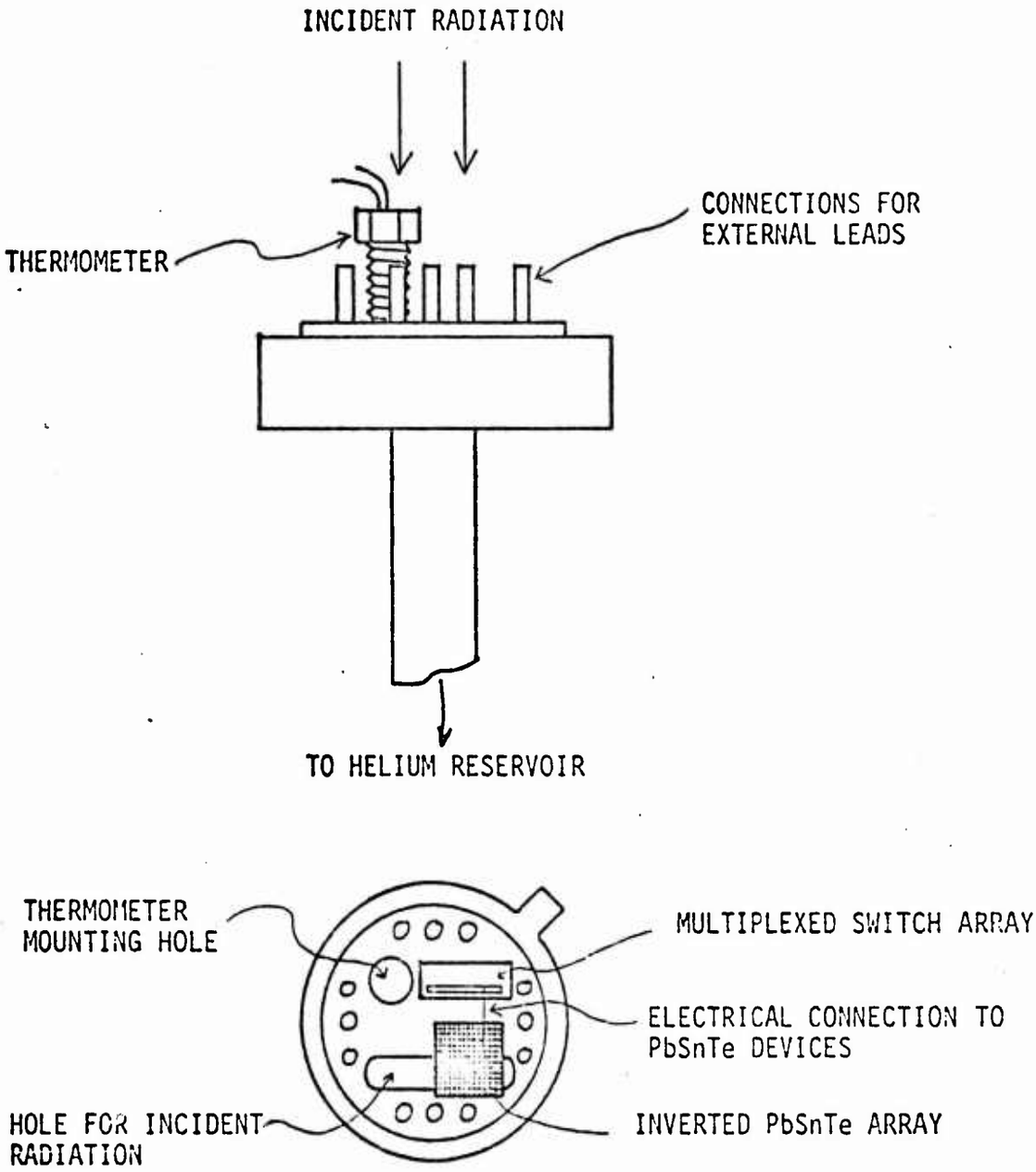


Fig. 17 Experimental arrangement used for experiments with linear multiplexer.

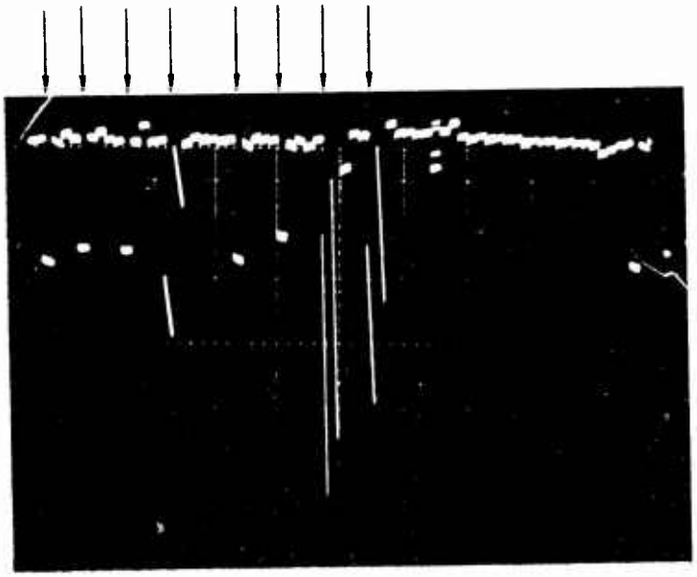


Fig. 18 Photograph of linear multiplexer output voltage waveform. Arrows show positions of PbSnTe devices wire bonded to the array. Sloping lines show the effects of leaky devices.

aperture and an attenuator restricted the photocurrents generated to less than about $6x10^{-14}$ amp for the 300°K background and about $6.0x10^{-12}$ amp for the 650°K background. The recharge amplifier circuit was identical to that shown for the previous experiment.

The output voltage was taken for a device with both the 300°K and 650°K background level. Recharge voltage level and frame time were then varied and the measurements repeated. Since the signal level for the 300°K background is too low to observe an output with the experimental setup used, the output is essentially that due to the 650°K background. This arrangement then simulates frame-to-frame subtraction operation since the leakage current contribution is cancelled out.

Evidence of charge storage operation can be seen in Fig. 19. Here, Δe_o, the recharge voltage difference is plotted versus frame time for V_r = -80 mV. The result is a straight line, within experimental error, showing no saturation behavior. This is exactly the result we would expect for charge storage operation with the signal levels used.

This is the first known demonstration of multiplexed operation of narrow-band semiconductor detectors operating in charge storage mode. The results presented here imply a minimum detectable current of $1x10^5$ electron/sec extrapolated to 2.5 sec frame time. Most of the noise responsible for this value is the result of the fact that the room temperature circuitry and interconnections to the low temperature dewar were not adequately shielded.

3.3 Silicon Multiplexer Acquisition

Prior to making the crucial decision about the final area array multiplexer to be purchased, a trial device was obtained to verify the design concepts to be included in the final multiplexer. This section discusses the properties of the trial device and measurements on that device which lead to the final multiplexer specifications.

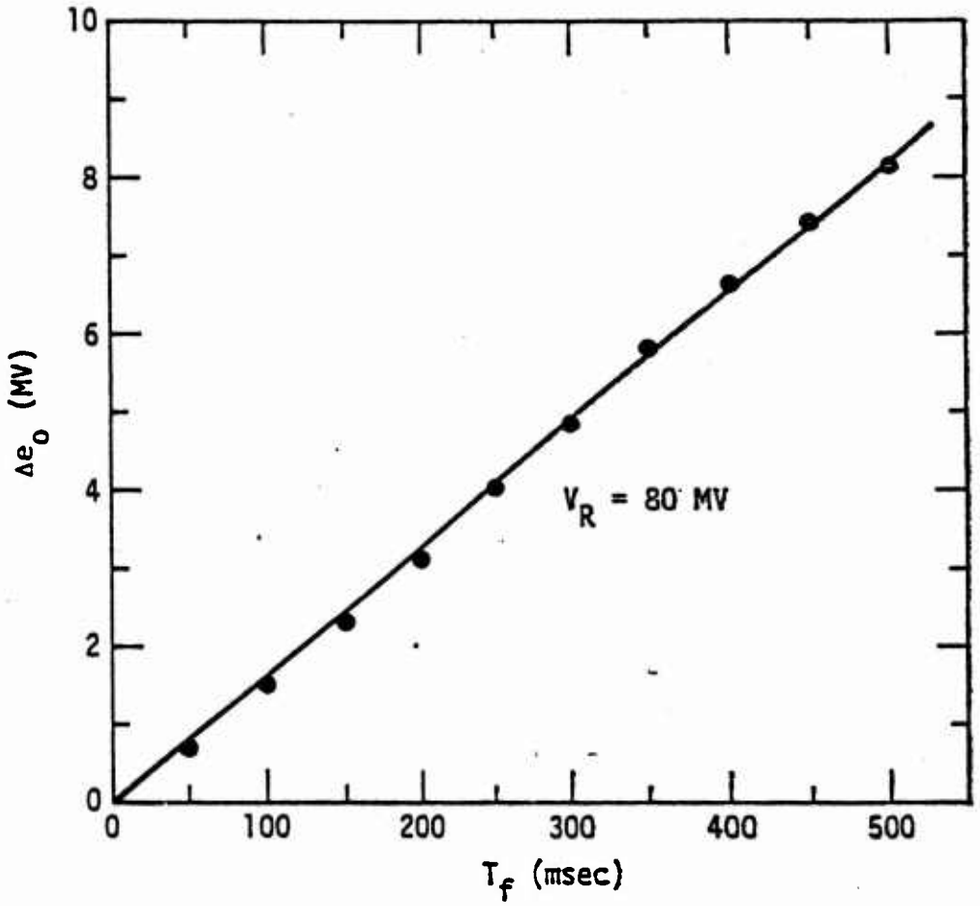


Fig. 19 Output voltage difference versus frame time for linear multiplexer charge storage experiments.

3.3.1 Custom Linear Multiplexer

Arrangements were made with Reticon Corp. to obtain some of their 64 element linear arrays modified so that we could inject signals into the source of the recharge switch FET. The linear multiplexer array was originally a visible and near infrared light sensor having an active photodiode area of 10x2 mils. Modification consisted of etching a via through the field oxide into the source diffusion of the recharge switch. This source diffusion originally served as the photosensitive element. Then a metal pad was applied over the source diffusion connecting into and through the via. The resulting metal pad was 10 mils by 1 1/2 mils and the metallization used was aluminum. Some measurements of the characteristics of the modified arrays were made at low temperature. Since the metallization did not entirely cover the source diffusion, the devices were somewhat sensitive to visible light and their continued operation could be checked by shining a light through the dewar window. Of immediate concern was the heat generated in the switch array. Initial tests in which the devices were operated with clocking pulses as were used in the Reticon circuits were rather discouraging. Lowest temperature of operation with the heat sinking used was greater than 30°K. This was with the heat sink temperature of 4.2°K. The temperature on the silicon chip must have been considerably higher since the thermometer was some distance from the array. The power dissipated was roughly equivalent to the Reticon specification of .125 watt. Since the PbSnTe devices would be directly connected to the silicon chip this was an unacceptable thermal load. Fortunately, an approach was developed which virtually eliminated the problem for the purpose of this electrical mating experiment.

A schematic drawing of the on chip circuitry including shift registers is shown in Fig. 20. PbSnTe diodes would be connected as shown conceptually by the dashed circuit elements in Fig. 20. The silicon source-to-substrate diode will be in parallel with the PbSnTe photodiodes. This

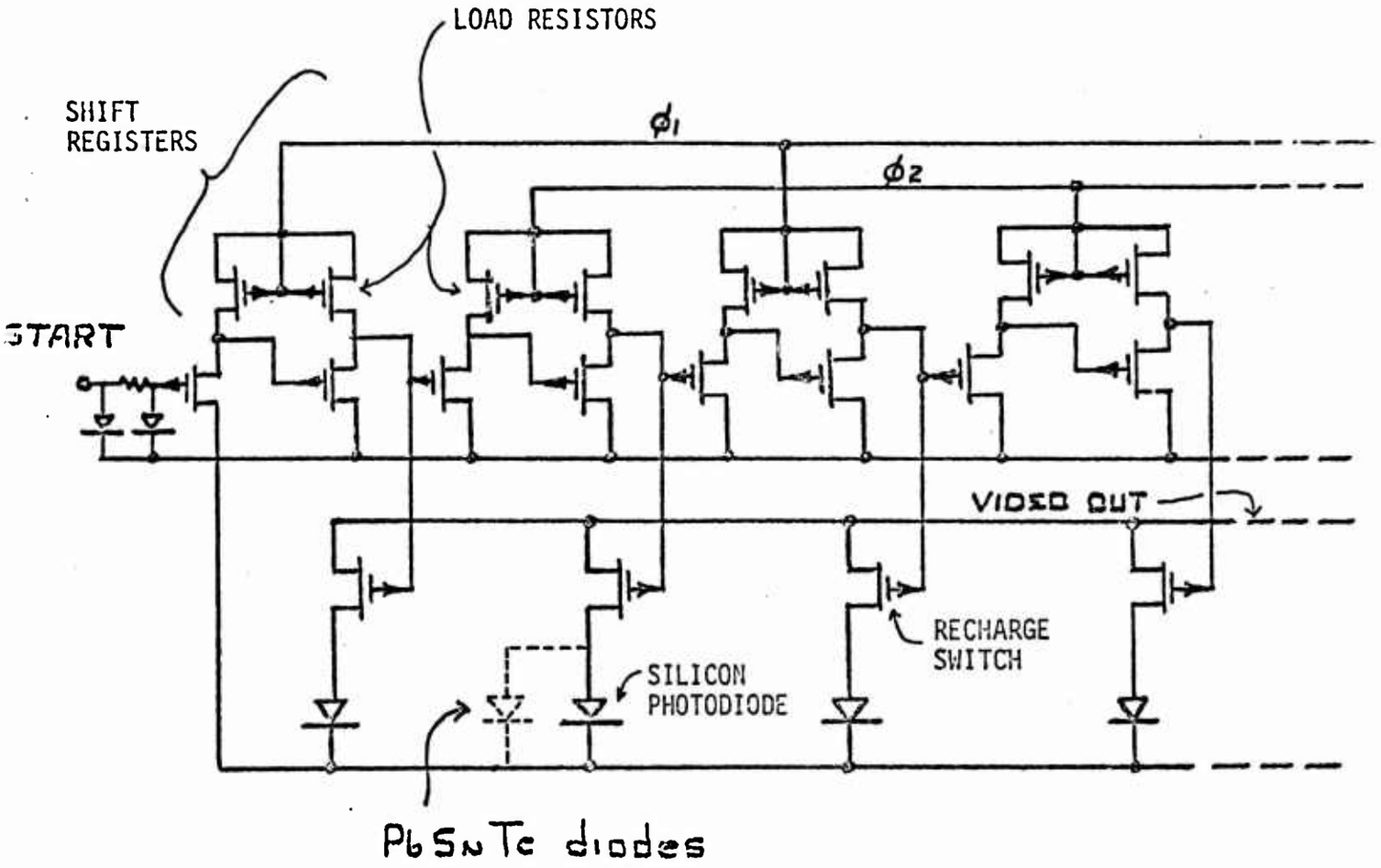


Fig. 20 Schematic electrical diagram of Reticon FET switch arrays. The dashed part of the circuit shows how the PbSnTe diodes will be connected in parallel with the silicon diodes.

is no problem because of the very low leakage in the silicon device particularly at the expected operating temperatures.

Nearly all the power dissipation in the switch arrays occurs in the shift registers which transfer the clocking pulses to serially address each recharge switch. Current flows through the FET transistors used as load resistors whenever a clock waveform (ϕ_1 or ϕ_2) is negative as shown in Fig. 20. Since ϕ_1 is on whenever ϕ_2 is off and vice versa, two load resistors out of every two cells at least, generate power. Therefore power dissipation is roughly independent of frame time since the length of the clock pulses is proportional to frame time. With this arrangement, the only way to reduce power is to lower the magnitudes of ϕ_1 and ϕ_2 as far as possible. However, when this was attempted, the changes observed in power dissipation were small.

A more straight forward approach is to reduce the length of the ϕ_1 and ϕ_2 pulse in time. In this case, the rise of one pulse is no longer coincident with the fall of the other. Then for fixed ϕ_1 and ϕ_2 pulse length, power dissipation should be inversely proportional to frame time. An experiment was designed to test these ideas. The original clock pulses and simulated video output is shown in Fig. 21 (a). Figure 21 (b) shows how the pulses were modified with the resulting output. The switching transients are not shown. Figure 22 shows the apparatus used. The cold end was surrounded by vacuum. A calibrated gallium arsenide diode thermometer measured the temperature of the header on which a custom switch array was mounted. The temperature of the array should be very close to that of the thermometer. Connections to the input and output pads of the array were made using a thermocompression bonder. Modification of the clock pulses was carried out using commercial multivibrator circuits triggered by the Reticon clock pulses. All switch array circuitry was external to the dewar and operated at room temperature.

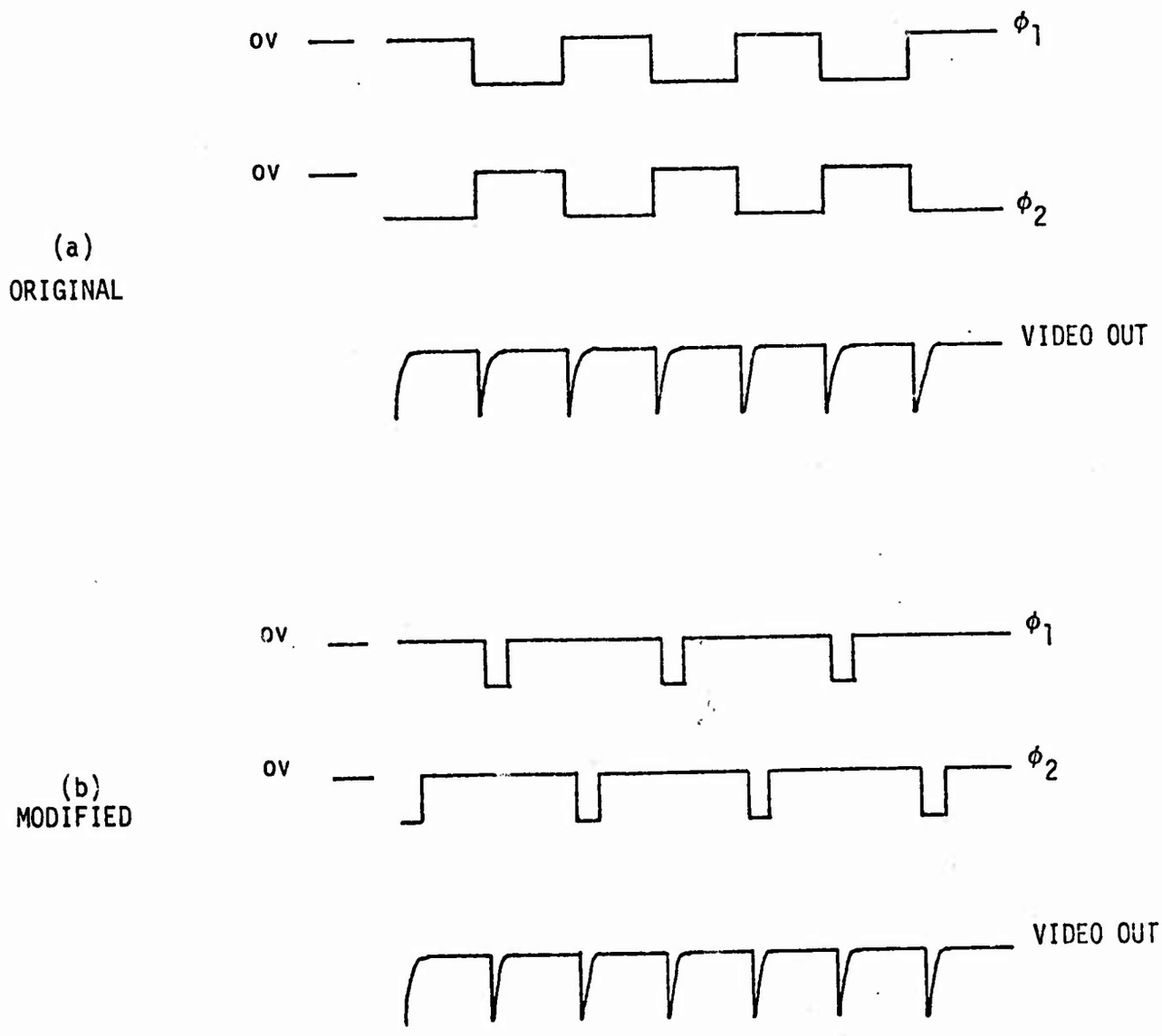


Fig. 21 (a) Clock pulses used in original clocking arrangement of linear multiplexer.
(b) Modified clock pulses designed to reduce power dissipation.

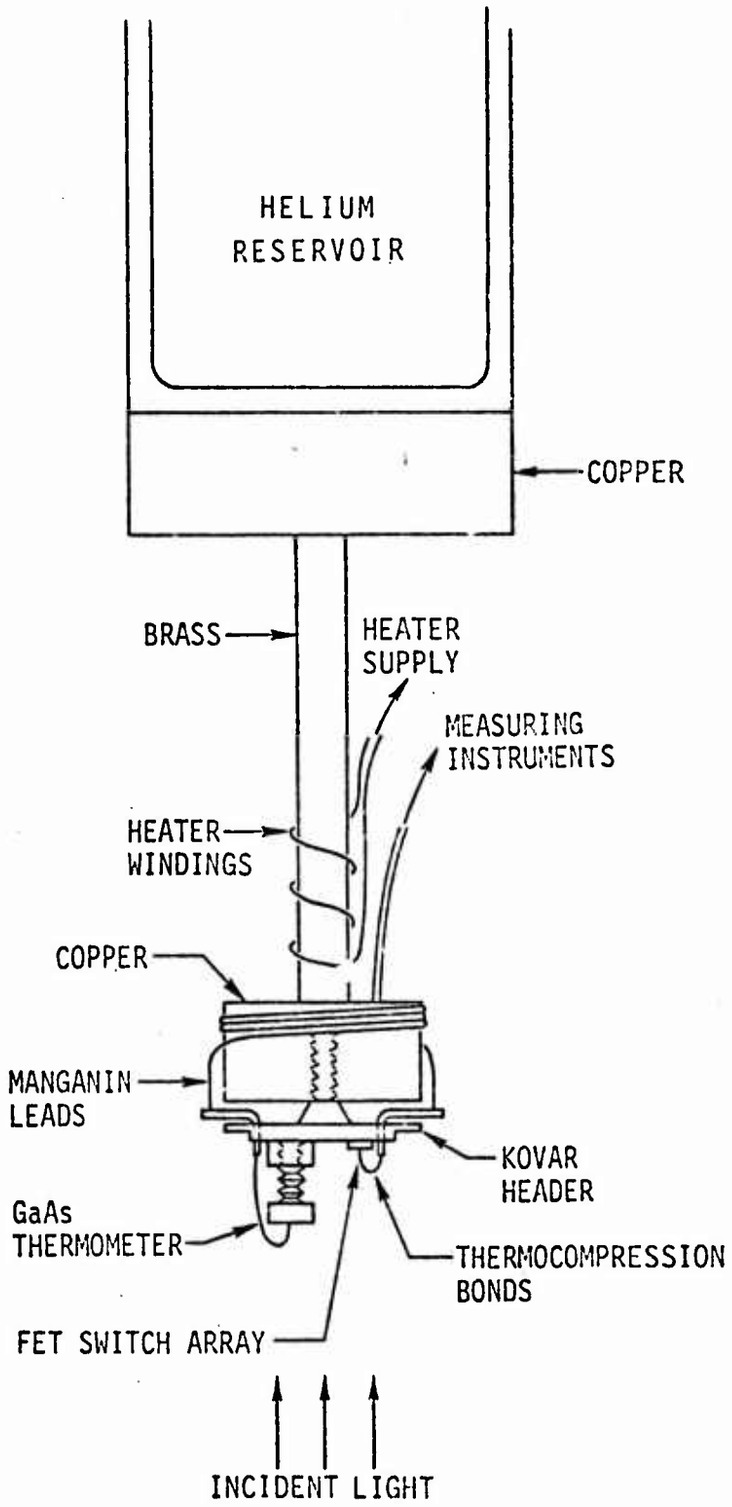


Fig. 22 Drawing of apparatus used for linear multiplexer power dissipation experiments.

Data was taken for three different frame times. For each value the temperature was measured as a function of duty cycle, defined as the ratio of the length of the clock pulse ϕ_ℓ to the frame time T_F. For the present arrays, frame time is 66 times the clock interval. The results are plotted in Fig. 23. In the initial experiment discussed earlier, the duty cycle, as defined above, was 50%. Here duty cycles are less than 1.5% and the resultant operating temperatures are much lower. Note that the curves for all frame times are virtually identical, indicating that power dissipation depends only on duty cycle. It also indicates that power dissipation in other parts of the circuit (e.g., terms proportional to $\frac{1}{2}\ C_{gs}V_g^2\ f_f$ in the recharge switches) are negligible for these arrays, since these terms are expected to be proportional to $f_f = \frac{1}{T_F}$. The fact that the experimental curves are not straight lines is not important because of the strong temperature dependence of thermal conductivities and heat capacities of the materials used in this temperature range.

Electrical operation at low temperatures was confirmed by the continued sensitivity to visible light. We did observe that as temperature was decreased below 50°K, silicon diode saturation occurred at lower light levels, indicating a decrease in photodiode capacitance. This is probably an indication of carrier freeze-out occurring. This effect is of no concern since the recharge switches continued to function.

These results are very significant. They meant that in any subsequent two-dimensional array power dissipation would be only a few microwatts for the entire array. This result would be achieved first by the reduction in duty cycle as just discussed, and also due to incorporation of new shift registers in which only one cell per shift register generated heat an any given time. As will be discussed in the next section, the power dissipation was in fact reduced well below this figure by additional innovations.

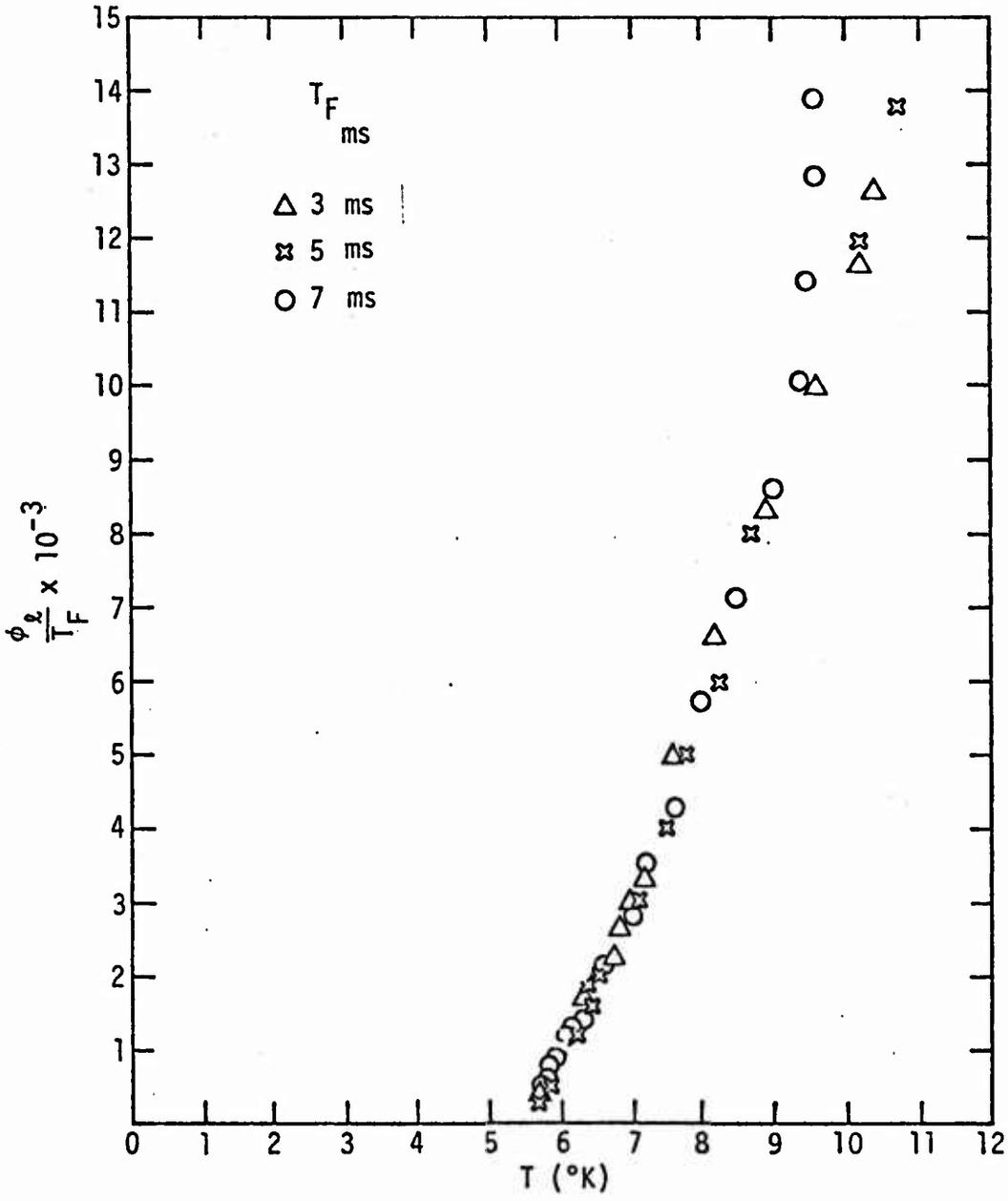


Fig. 23 Plot of array temperature versus duty cycle for linear multiplexer power dissipation experiments.

The second major area of concern regarding the Reticon multiplexers was the material used for the bonding pad. Since Reticon was unwilling to depart from the standard metallization procedure in which only aluminum is utilized, it was necessary to accept that metal on contact pads. The problem was that thermocompression bonds could not be made to the aluminum because of the oxidized layer which formed rapidly after fabrication. Since the pads were only 1.5 mils wide, any attempt to increase heat and pressure during bonding resulted in smearing of the gold wire onto the adjacent contact pads. Our original efforts to solve this problem were to bond by sputter etching the aluminum pads - thereby removing the oxide which had prevented bonding. This worked well only if the bonds were made immediately after etching. The oxide reformed very rapidly. To overcome this, a mask was made so that photoresist could be applied except over the pads. Then the sputter-etching was carried out and in the same chamber, 200Å of chromium and 400Å of gold was sputtered over the entire surface. When the photoresist was removed, the applied metal lifted except on the pad. Bonds could then be made to these modified pads at any time after application. This processing development was critical and would be successfully applied later in this development for proper contact to the aluminum pads on the area multiplexers. In fact, successful application of this procedure means that any silicon chip processed with standard techniques can be modified on our laboratory to provide low impedance interconnects into appropriate parts of the circuit.

3.3.2 Area Array Multiplexer Modifications

As a result of the measurements on the linear multiplexer, discussions were held with Reticon Corp. concerning reduction in power of the shift register. Normally this is not a serious concern with Reticon because most of their devices are operated at room temperature and in an environment in which power dissipation is irrelevant. Initially

it was agreed that the shift registers would be the same as in their standard 32x32 element visible sensor array. These shift registers were described in the last section; only one cell of each shift register dissipated power at any given time. Combined with the new clocking arrangement discovered with the linear multiplexers, the power dissipation would then be approximately a few microwatts. This of course, was strictly true only if the pixel time were the same as in the study on the linear multiplexer. However, due to the larger number of pixels in the array multiplexer, the power dissipation would have, in fact, been boosted to approximately 100 microwatts. Since the PbSnTe devices would be connected directly to the silicon chip not by wire bond as in the previous case this amount of power dissipation might seriously degrade the cold finger operating temperature. Therefore, it was felt that a lower power shift register should be sought.

As a result of our discussion, Reticon supplied to us an experimental linear multiplexer incorporating a new shift register which omitted the load resistors that were the major source of power dissipation in the older design. Our tests showed that indeed this shift register worked well and operated at low temperature with minimal power dissipation. The decision was made to incorporate these new shift registers into the 32x32 imager chip. Additional modification to reduce power dissipation was to bring out additional pads which by-passed the gate protection resistors. These gate protection resistors were a source of power dissipation becasue all clock pulse current was fed through them. The new design was to incorporate pads which would allow us to select or not to select as we wished the gate protection resistors. Still another source of power eliminated were the resistors associated with self start features on the standard product. These modifications would theoretically yield a reduction of power dissipation to unmeasurable proportions. In fact, no subsequent experiments were able to detect any

temperature rise in the multiplexer mount. The problem of power dissipation in this type of multiplexer was completely solved.

Additional modifications to the multiplexer dice included the incorporation of metal pads and vias connecting the pads to the FET recharge switch source diffusion. This pad is shown in Fig. 24 (b). Figure 24 (a) shows the appearance of the unit cell in the standard product. Again this pad was aluminum.

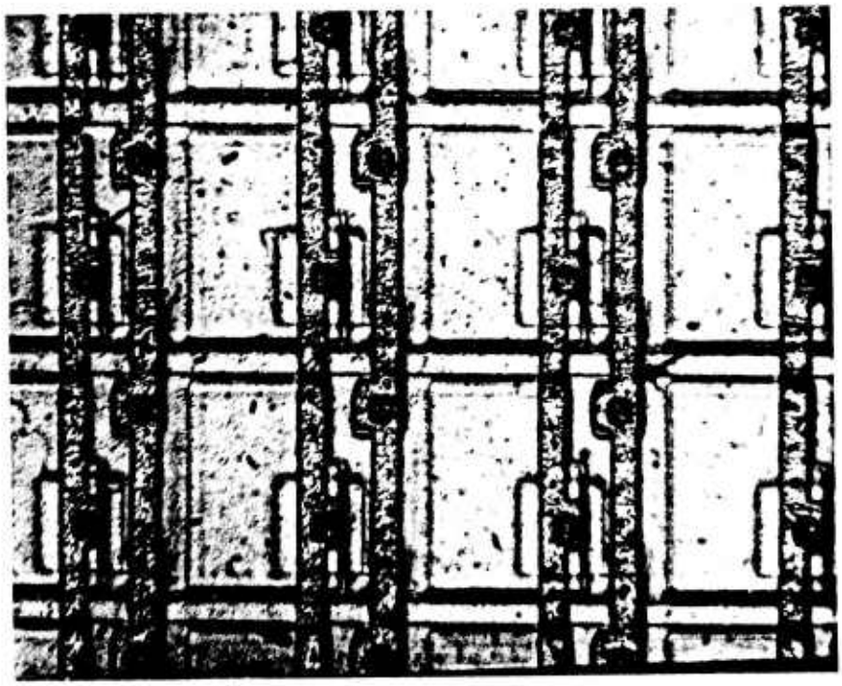
Another modification to the standard procedure was to utilize silicon wafers which were polished on both sides for the processing. This enabled the use of an infrared microscope viewing through the backside of the chip for the purpose of mating to the photodiode array. (Standard procedure was to lap the substrate on that side but tests showed that an image could not be obtained through such a lapped surface.) Ultimately 60 dices with these modified features were obtained from Reticon.

3.3.3 Multiplexer Driver Construction

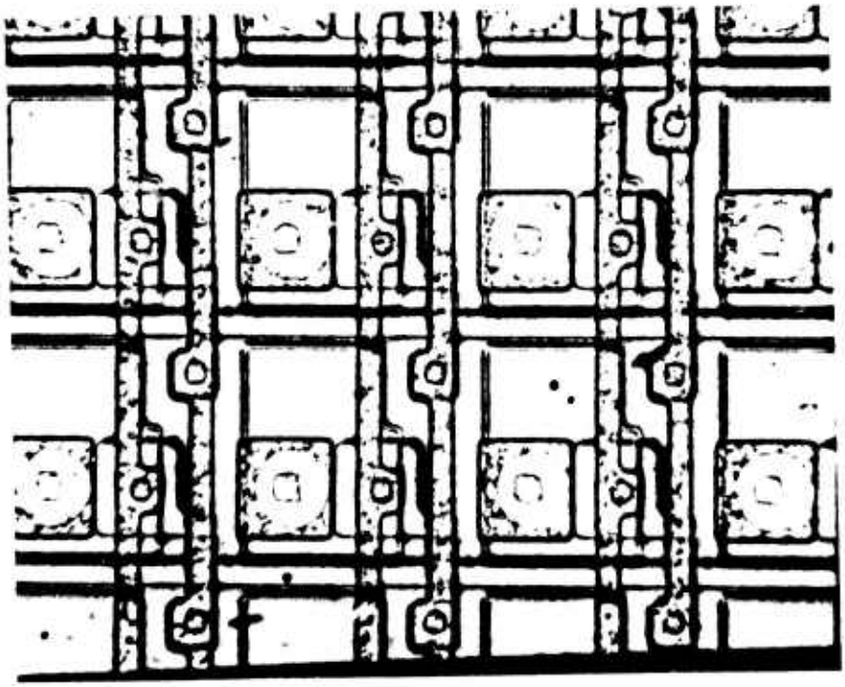
Because of the unique requirements on multiplexer operation for this program, it was necessary to custom design the drive electronics for the multiplexer. After several arrangements were constructed, the final design evolved into a highly usable, flexible circuit. In this circuit one could obtain independent variation of clock pulse width, amplitude, frame time, and spacing between clock and reset pulses.

3.3.4 Minicomputer Interface

The original proposal for this program referred to the usefulness of a computer acquisition of data from the multiplexed arrays. This was deemed necessary because of the large number of devices to be interconnected. In fact, experience has shown that the computer interface is critical for the determination of device parameters across the entire array. Because of delays in implementation of our laboratory minicomputer system, the interface to the complete arrays was not constructed in time



(a)



(b)

Fig. 24 (a) Photograph of unit cell of standard Reticon 32x32 element multiplexed array.
(b) Photograph of unit cell as modified for this program.

for this program.

Actual construction of such an interface is nearing completion at this time on IR&D funding.

3.4 Interconnect Development

This section deals with the development of the process used to fabricate the interconnects between the photodiode chip and the silicon multiplexer chip. The properties of the two chips have been discussed earlier in this report and the interconnects represent the third major aspect of the hybrid focal plane problem.

Because the theoretical considerations with respect to interconnect geometry were covered in Section 2.2.3, the discussion below relates to the techniques for achieving the desired geometry and uniformity of the interconnects.

3.4.1 Methods of Interconnect Fabrication

Many methods have been proposed and, indeed, been utilized for the fabrication of metallic interconnects. The method chosen for this development is electroplating. This method has several unique advantages and is relatively cost-effective. Alternate techniques and the reasons for rejection are summarized in the list below.

1) Ion milling from thick film: This method was not considered feasible because of the very high aspect ratio interconnects needed for this development. In addition, the effects of the ion milling process on the underlying MOS circuitry of the multiplexer chip are uncertain. No experiments were carried out during

this program, but results of other workers have shown that the ion milling of indium is very slow and therefore is not cost-effective for future technology applications.

2) Evaporation through metal mask: Some experiments were carried out, but it was found to be an impractical method for two reasons. First, unless the mask was in contact with the interconnect base plane, metal was deposited under the mask to the side of the intended deposition region. This would eventually result in shorting of interconnects. Second, because deposited metal built up around the holes in the mask, their diameter became smaller as the deposition proceeded. The maximum practical deposition at one time was perhaps 0.5μm for these reasons. Therefore, a 50μm high column would require 100 evaporations through clean masks. The cost of this procedure would be enormous.

3) Sputter-etching from thick film: Rates of etching indium are acceptable for this application, but undercutting during standard sputtering procedures would prevent proper interconnect definition. No experiments were tried with plasma etching which would potentially result in less undercutting because of difficulty in masking and in protection of the underlying MOS circuitry.

4) Wet chemical etching from thick film: Not practical because of undercutting.

5) Placement of preformed interconnects or spheres: Placement of small indium or solder spheres has been used successfully in the past for flip-chip interconnects on silicon circuitry. However, at least two spheres, one on top of the other are needed to achieve the required aspect ratio here. Also, previous work was done with considerbly larger spheres than the one mil diameter needed here. Placement of preformed columns was not considered practical for large scale applications.

6) Casting of interconnects: Several methods of casting interconnects have been studied. The advantage of casting is that all the interconnects are made at once. The disadvantage is that it is difficult to make the mold. Once an array of columns is cast and demolded, it should be possible to mount multiplexer die to the columns (supported by a base of bulk metal) and to subsequently remove the metal base and mount the photodiode array. Conceptually, the process seems promising, especially for high volume. However, in practice it proved to be difficult to fabricate the mold. After a few attempts with laser drilling, this approach was not pursued: In this same category is the possibility of extruding interconnects through a die. Although feasible, the die is difficult to make and the processing steps to transfer interconnects are formidable.

Taking into account the above considerations, electroplating is the method chosen. Indium is easily electroplated from standard solutions. By plating through holes in photoresist, the lateral dimensions of the interconnects are controlled. In addition, plating results in a clean surface, necessary for cold welding, as will be discussed later.

The plating solution used is standard indium sulfamate solution obtained from Indium Corporation of America. Plating results were consistent when fresh solution is used. Evaportation of water from baths left open for more than a day resulted in dendritic growth. Because of the small quantities used, the baths were replaced with fresh solution just before each plating operation.

Despite the acidity of the plating solution, it was found that Shipley AZ 1350-J stood up well to the solution. However, in thicker resist layers, exposure to plating solution seemd to accelerate cracking of the resist around interconnects if it became excessively dry.

Therefore, the scheduling of process steps became an important matter to ensure that the resist remained sufficiently flexible. The details of the processing of high aspect interconnects are left to the next few sections.

3.4.2 High Aspect Ratio Interconnects

A design goal for the interconnects is an aspect ratio of two. That is, the height of the columns should be 50μm for a diameter of 25μm. Since the theory of the mechanical properties of indium interconnects is rather coarse, these numbers should be taken as nominal values. As will be seen, an ideal cylindrical geometry is difficult to achieve, so the numerical aspect ratio gives an approximation to the actual geometry. In practice, the aspect ratio obtained is determined by estimating the diameter of the column looking down from the top in a high power microscope. By focussing first on the interconnect base and then on the top of the interconnect, its height is determined. This measurement always gives an underestimate of the aspect ratio since the view from the top shows the widest cross-section. Also, when resist surrounds the column, its higher index of refraction reduces the apparent height. The SEM can be used to give more accurate aspect ratios, but it was rarely used because MOSFET gates on the multiplexer did not survive the high energy electron beam.

In order to fabricate high aspect ratio interconnects, it was necessary to make some adaptation of standard resist processing techniques - techniques that are ordinarily most suitable for two-dimensional processing. This adaption turned out to be one of the most difficult aspects of the program because only contact mask aligners were available at the time.

The process used to fabricate high aspect columns consists of repeated resist application and electroplating. An interconnect pad is provided at the desired position of each interconnect. Fabrication

of the interconnect pad varies according to the type of silicon chip used, as will be discussed in later sections.

The process sequence for interconnect fabrication is contained in the list in Table 1. It is assumed here that an adequate interconnect pad is provided on the chip. More specific discussion of these steps follows in the next two sections.

3.4.3 Growth of Interconnects on Test Chips

3.4.3.1 Description of Test Chips

In order to begin development of the interconnect processing prior to receipt of the multiplexer dice, a test chip was designed and fabricated at the Science Center. Silicon wafers 2" in diameter and 0.12" thick were purchased polished on both sides. These were then coated on both sides by sputtering with 1500Å of SiO_2. One side was then coated with 100Å of titanium and about 5000Å of gold. Then the wafer was diced into 1/2" x 1/2" pieces and a pattern of lines etched through the gold. The pattern is shown in Fig. 25. When an array of one mil diameter interconnects on 4 mil centers is superimposed on this pattern, 124 of the interconnects lie uniquely on gold lines that are isolated from ground. The remaining 900 interconnects all lie on lines which are permanently grounded. Then the devices connected to the single element striplines may be individually accessed by probing or wire bonding the corresponding lines. The stripline pattern is shown in more detail in Fig. 26.

The single element striplines can be shorted to ground, for plating purposes, at their outer ends if a conducting material is applied to the proper area of the chip. Since the single element striplines have grounded lines on both sides as shown in Fig. 27, grounding can be easily accomplished with a conducting material.

3.4.3.2 Interconnect Growth

After fabrication of the test chip with stripline pattern, photoresist (Shipley AZ 1350J) is applied approximately 10μm thick.

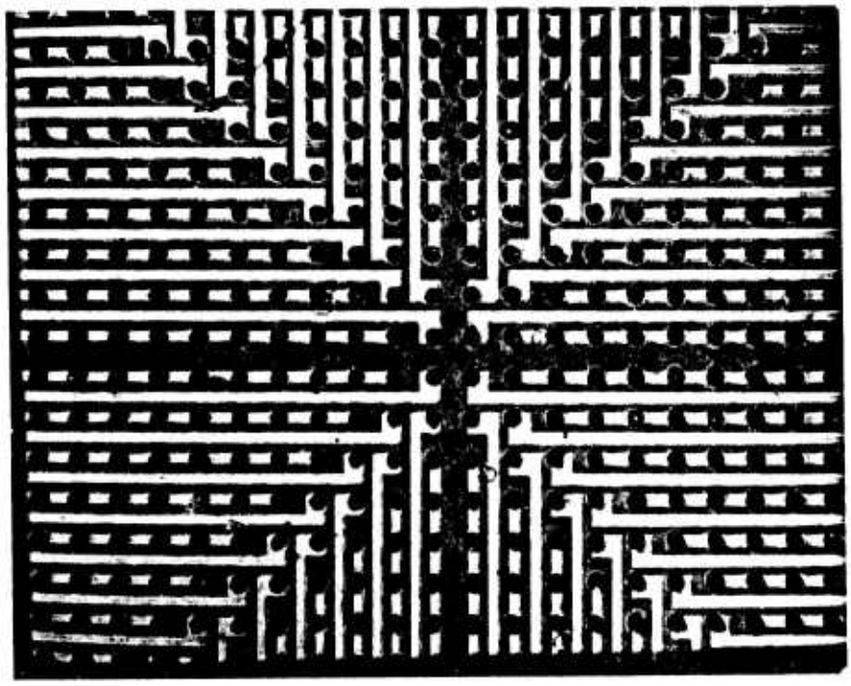


Fig. 25 Test chip stripline pattern.

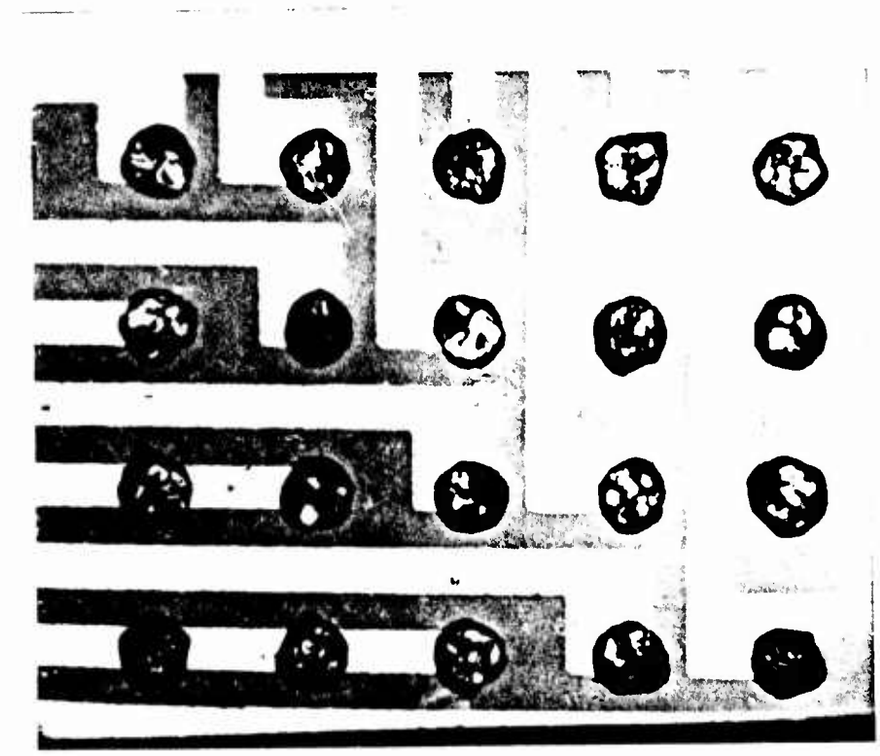


Fig. 26 Detail of test chip stripline pattern.

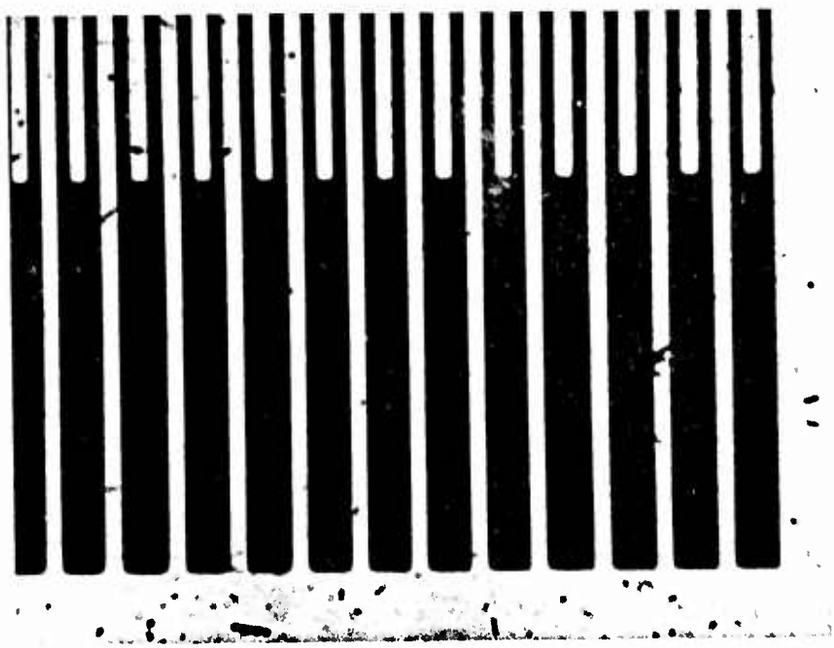


Fig. 27 Detail of grounding end of test chip stripline pattern.

TABLE 1

HIGH ASPECT INTERCONNECT PROCESS STEPS

1. Apply photoresist mask which defines interconnect diameter and positions.
2. Electroplate indium through mask to a height at which the diameter just begins to increase.
3. Remove mask with solvent.
4. Apply resist using more than one coat if necessary to obtain coverage of interconnects.
5. Open holes through resist down to the top of previous column increment.
6. Electroplate next increment of height until diameter just begins to increase.
7. Repeat steps 3 through 6 until desired height is obtained.
8. Final electroplating is continued until column extends approximately 10μm beyond top of resist.
9. If chips are not used immediately for mating, they are placed in the plating bath and an additional thin layer of indium deposited immediately before mating.

Thickness of applied resist is dependent on resist viscosity and on spinning speed. Control of thickness is accomplished by controlling these factors.

Holes are then opened through the resist at the desired interconnect positions by means of a dark field iron oxide mask. It is found that very well-defined holes can be made through the resist up to about 10μm thick with the exposure system used. During this same exposure, the areas around the ends of the single element striplines were also opened.

After mask definition, chips were mounted on a glass slide and alcchol dag used to short the single element lines by painting across the opened areas. When silver paint was used to short the lines, the large grain size apparently resulted in some lines not being adequately shorted. This caused uneven plating.

At the same time the dag was applied, a thin wire was attached to the ground plane and run up the glass slide. After baking the mounted sample at 95°C for 10 minutes to dry the dag, the entire chip, exclusive of the region containing the interconnects was coated with an insulator to prevent spurious plating. If spurious plating was observed, the sample was removed from the plating bath and touched up with the insulator.

In the case of the test chips, the gold striplines formed an adequate interconnect base. So it was only necessary to dip the mounted chip in plating solution and apply a potential to the thin wire. Commercial indium sulfamate solution was used and the anode was pure platinum.

In some cases, it was found that initiation of the plating was improved by passing a large current through the plating bath momentarily. This was accomplished by discharging a capacitor. However, too large a current flow resulted in lifting and fracturing of the resist around the interconnect base. Therefore this "striking" procedure was used only when it was apparent that plating was not beginning uniformly. Any

sample that plated uniformly from the very beginning invariably yielded very uniform interconnects throughout the remainder of the process.

Plating was carried out at a current level of approximately $3x10^{-6}$ amp per interconnect. After about two hours, depending on the thickness of the resist, the columns had reached the top of the resist and begun to bloom out. At this point, the chips were removed from the glass slide by soaking in acetone. This also removed the photoresist on the chip, but did not remove the dag.

The next increment of interconnect height was applied by repeating the process described above. However, photoresist application was done in several steps. It was found that the best procedure was to apply a first coat with low spin speed, then bake, then increase the spin speed with each subsequent application. This was continued until the resist was about 10μm over the top of the existing columns. The resulting photoresist surface was nearly planar.

Exposure of the resist over existing columns proved to be very difficult, particularly as the height was increased. Because the photoresist and the iron oxide mask apparently had their maximum spectral transmission at somewhat different wavelengths, the poor contrast ratio made it nearly impossible to align the interconnect hole pattern to the stripline structure when the resist was thicker than about 30μm. Under these conditions, the tops of the interconnects were used for alignment. However, the columns had some curvature at the top surface, so the reflectivity was reduced. Only by focusing on the column top with high magnification could its position be accurately discerned. Then, of course, the mask pattern was out of focus because of the 10μm height above the interconnect. With practice it was possible to obtain good alignment on most attempts.

An additional problem related to photoresist exposure was the damage caused by contact of the mask to the photoresist when tall interconnects were involved. Since excessive drying of the resist

caused cracking, exposures were done while the resist was rather soft. Therefore, the standard procedure of pressing the sample against the mask could not be used because even gentle contact resulted in fractured resist and interconnects. A Cobilt mask aligner was modified so that the sample holder could be raised mechanically in small increments until sample and mask were almost in contact. Divergence of the exposure beam in this aligner was small enough to yield good hole definition through 10μm of photoresist even when there was no mask contact.

Development of the exposed photoresist was carried out for at least 60 seconds with full strength Shipley AZ 1350J Developer. One hundred percent inspection of the interconnects was essential at each phase of the processing. Usually, incomplete exposure or development could be repaired if discovered immediately.

It was never necessary to repeat the "striking" procedure during plating of the second and subsequent interconnect increments. If the first increment plated uniformly, the remaining increments would inevitably plate uniformly.

The last increment of plating is continued until the indium blooms out well above the photoresist. This produces a bump for mating to the photodiode array. All of the deformation of the interconnect which occurs during mating is accommodated by this bump. Any variations in photoresist height or deviations from flatness of the photodiode chip can also be accommodated. This will be discussed more fully in Section 3.6.

3.4.3.3 Results of Plating Experiments

Prior to obtaining uniform arrays of interconnects, several problems were encountered and overcome. The following list summarizes these problems and their solutions.

1. Non-uniform plating due to inadequate single element stripline grounding: Solved by use of alcohol dag instead

of silver paint. Some problems still remained and were identified as due to insulating photoresist being applied before the dag was adequately dry. Apparently the carbon particles in the dag separated and were insulated by the resist. A more careful drying schedule prevented reoccurrence.

2. Non-uniform plating due to excessive stripline resistance: Because the striplines differ in length, the plating current will not be divided uniformly unless the line resistance is small. This was a problem in some cases in which the lines were not thick enough. This was solved by using a thicker gold deposition prior to etching the striplines.

3. Indium plated dendritically: This was caused by evaporation of water from the plating bath and was solved by using fresh solution daily. The denritic growth distorted the column profile and, because of the high reflectivity of the crystallite planes, subsequent resist exposure was very irregular.

4. Non-uniform plating initiation: Occasionally at the beginning of plating on a fresh interconnect base, all of the interconnect positions did not initiate. Once initiated the indium will plate easily. However, if an interconnect base does not start plating at the same time as those around it (because of some contamination or other mechanism) it will not plate at all because the current will be shunted to those that already have an indium deposition. This was solved, when necessary, by the "striking" procedure already described. Even more helpful is a procedure in which the sample is drawn repeatedly through the bath meniscus.

Although the exact cause is not understood, this procedure is very helpful in effecting uniform plating initiation, even for samples for which striking was not successful.

Despite the fact that uniform arrays of interconnects were obtained, the test chip was not a completely acceptable simulation of the hybrid structure. This was primarily because only about 10% of the interconnections could be checked for continuity and device characteristics and because the plating was accomplished thorugh striplines whose geometry varied depending on the position of the interconnect. Despite these drawbacks, the procedure for high aspect interconnects was developed with the test chips and mating experiments resulted in a demonstration of the hybrid structure as will be discussed in later sections.

3.4.4 Growth of Interconnects on Multiplexer Dice

This section deals with the fabrication of high aspect ratio interconnects onto the silicon multiplexer dice obtained from Reticon Corporation. The general details of interconnect growth were contained in the last section, so the ensuing discussion will consider those difficulties which are unique to the multiplexer and those procedures which had to be modifed.

3.4.4.1 Multiplexer Die Mounting

Because the test chips were large enough for easy handling, it was not necessary to mount them in auxiliary holders. The multiplexer dice required mounting for three reasons. First, handling of the individual dice often caused chipping and malfunction. Second, holding the processed dice in the mating apparatus was facilitated by the special mounting package. Finally, by carefully designing the package, it was possible to apply photoresist to the dice without the buildup around the edge normally encountered with small chips.

The design of the special package is illustrated in Fig. 28. The die is held in a cavity so that its upper surface is flush with the package surface. When photoresist is applied and the assembly spun, there is no edge buildup on the die due to surface tension of the liquid resist.

A hole is provided below the die for viewing through the die during mating. Mounting holes on the package are used for attachment to the mating apparatus and the mounting to a header for measurement. The original design of the package included insulated striplines fanning out from the multiplexer die to facilitate electrical connections to the die. However, due to difficulties in fabrication of these lines, the striplines were eliminated and subsequently wires connected to multiplexer were looped from the die directly to the mounting header pins.

Mounting of the dice was accomplished with silver-filled epoxy, Epo-tek 415G, manufactured by Epoxy Technology.

3.4.4.2 Interconnect Pad Fabrication

Because the multiplexers were obtained from Reticon Corp. the only material available for metallic connection to the access switch source diffusions was aluminum. Initial experiments showed that the aluminum oxide which formed on the pads prevented uniform plating of the indium. Therefore, a procedure was developed to remove the aluminum oxide and apply a gold pad to be used as an interconnect base. Gold was also applied to the signal and clock access pads. After mounting a die in the package described above, the following procedure was used:

1. Apply AZ 1350J photoresist and open holes over interconnect and access pads. Bake only 5 minutes at 95°C.
2. Place samples in RF sputtering system.

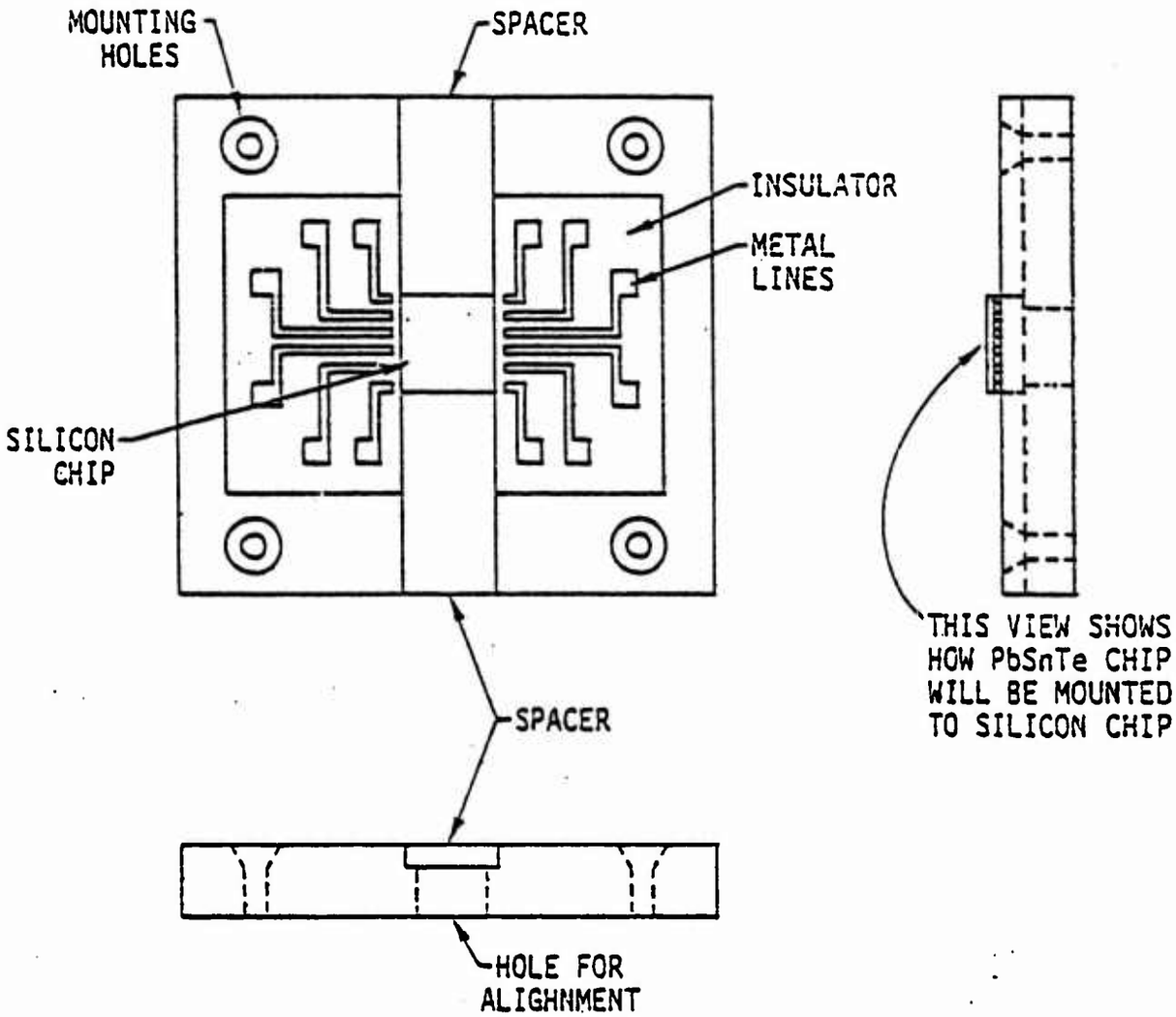


Fig. 28 Drawing of multiplexer die holding package.

3.4.4.3 Interconnect Growth on Multiplexer

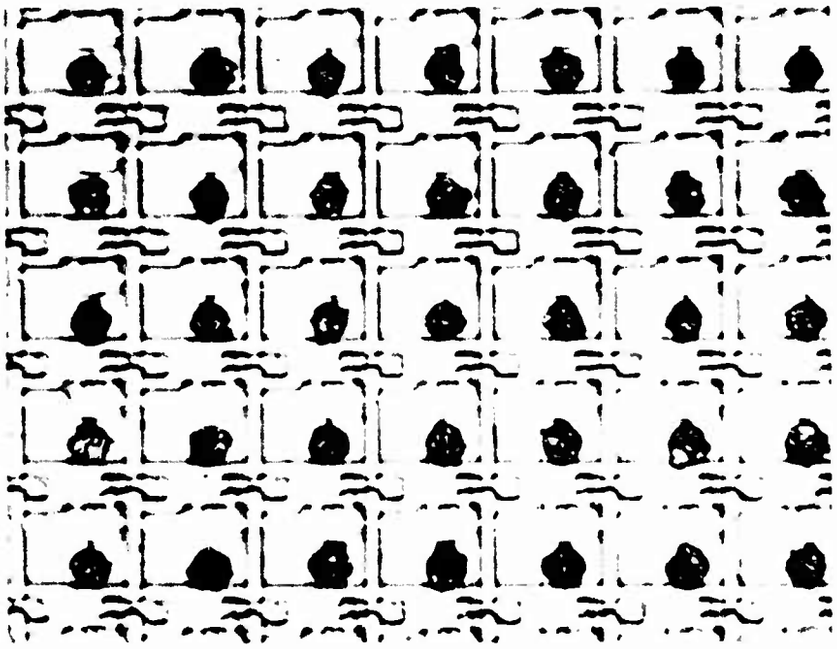
The growth of the interconnects onto the multiplexer dice was carried out in essentially the same way as described for the test chips in Section 3.4.3 with two exceptions. First, the plating current is passed through the metal package, the silver-epoxy and the multiplexer substrate. Therefore each interconnect pad is at the same potential resulting in much more uniform plating characteristics.

The most important difference is that the interconnect pads are in contact to the p^+ access switch source diffusion. Therefore the plating current passes through a p-n junction at each interconnect site. Fortunately, the direction of current flow is so as to forward-bias this junction. For an n-channel multiplexer, it would have been necessary to short the interconnect pads temporarily with a ground plane or to clock the array and pass charge through the video line. Neither of these undesirable contingencies was necessary.

Figure 29 shows a photomicrograph of a multiplexer with an array interconnects. The large crystallites characteristics of electroplated indium can be seen in the figure.

Several serious problems relating to interconnect growth were encountered and overcome. In addition to those encountered during the test chip work, the program was plagued with an additional difficulty associated with the multiplexer. This was the result of exposed clock lines on the multiplexer dice.

For reasons still not confirmed, progressive degradation of exposed aluminum metallization occurred as the processing of a die proceeded. This appeared as dissolution of random areas of the



ELECTRICAL AND PHYSICAL MATING TO SILICON MUX

INDIUM INTERCONNECTS FABRICATED ON SILICON MULTIPLEXER CHIP

Fig. 29 Photomicrograph of part of an array of interconnects fabricated on a multiplexer die.

exposed aluminum. Tests to determine the cause showed that exposure to silver-epoxy, photoresist, photoresist developer, indium plating solution and acetone individually could not reproduce the observed damage. However, silver epoxy and photoresist applied together and then baked did cause some damage which was similar to that observed during processing. Although this is not conclusive, there was a possibility that some of the silver epoxy was freed during lifting of the gold to form the interconnect pads. If small particles adhered to the aluminum, a catalytic action could have resulted in degradation during photoresist curying. The problem was alleviated somewhat by switching from Eop-tek 410E originally used for die mounting to 415G as noted above. However, this did not completely solve the problem. Because the degradation was progressive, more than half of the batch of 60 multiplexers purchased were affected by the problem. In some cases, the degradation appeared to continue even after a device had been mated and initially clocked. In these cases, the clocking abruptly stopped and visual inspection showed the cause to be a break in a metal line.

Although the process added considerable time to interconnect fabrication, it was decided to protect the lines on the remaining dice with a layer of pyrolytic SiO_2 (silox). An initial attempt at sputtering SiO_2 resulted in destruction of MOS gates on the multiplexer. The silox worked very well. A mask was made to allow etching of the silox over the access pads and the interconnect mask was used for the interconnect pads. Etching of the silox was done with buffered HF through a mask of AZ 1350J baked for 5 minutes at 105°C. In no case did excessive undercutting of the silox layer result in damage to the multiplexer circuitry. No multiplexer degradation whatsoever occurred after this procedure was initiated. Also, the silox layer gave considerable protection against mechanical damage to the metal lines.

3.5 Development of Mating Techniques

This section discusses the techniques developed to position the photodiode chip relative to the multiplexer and to join them together.

3.5.1 Mating Apparatus

An apparatus was desitned and constructed which was capable of manipulating the photodiode and multiplexer chips and mating them together. A photograph of the apparatus is shown in Fig. 30. The photodiode chip is held by gravity, mesa side up, on a metal block fitted with a small steel ball in the underside. This ball sets in a socket so that the photodiode chip will level itself when pressure is applied during mating.

When the test chip is used, it is held above the photodiode chip in an annular vacuum chuck surrounding a hole through which the alignment of the two chips is observed. An infrared microscope is used to view through the silicon chip. The photodiode mesas can easily be seen and the distance between chips measured.

The photodiode chip can be translated in three perpendicular directions and the angle of the silicon chip can be adjusted around three orthogonal axes. Since the entire mating apparatus is constructed on the stage of the infrared microscope, the two chips can be moved simultaneously under the microscope eyepiece using the stage maniuplators. A strain gauge on the photodiode holder measures the total mating force.

When the multiplexer is being mated, it is attached to the apparatus by the holes provided in it special mounting package.

3.5.2 Mating Procedure

The procedures for mating photodiode arrays to the test chip or to the multiplexer are essentially the same. After preparation of the photodiode array it is paced on the swivel block described above and the test chip or multiplexer is mounted in its position above the photodiodes. The silicon element is leveled by viewing each corner repeadtedly with the microscope high power objective. The photodiode array is leveled by bringing it up gently against a flat part of the multiplexer package or test chip ground plane. Then the two chips are brought slowly together maintaining a slight separation.

Fig. 30 Photograph of mating apparatus

Viewing through the test chip is quite easy because of the SiO_2 layer on the back side which serves as an anti-reflection coating for the incident infrared light. Because of possible damage to the multiplexer due to the additional process steps, a similar coating was not applied. This made alignment of the multiplexer somewhat more difficult since the spurious reflected light from the back side of the silicon reduced the contrast ratio for viewing the photodiodes. This problem could be alleviated greatly by polarizing the incident light.

Continuous adjustments of the relative lateral positions and azimuth of both chips are made as they are brought gradually together and finally into contact.

3.5.3 Cold Welding

For a number of reasons, it was decided to use a cold welding technique to join the two chips rather than a reflow holder process. These reasons are as follows:

1. It would be difficult to maintain a high aspect ratio interconnect by reflow.
2. Damage to device characteristics might result if subjected to the temperatures necessary to melt indium and lower melting alloys do not have the proper mechanical properties.
3. Indium is used for the interconnect material and it is nearly ideal for making cold welds.
4. Tests showed (see discussion of results) that detector characteristics were not degraded by the force required for the cold weld.

In order to make the cold weld, a force of approximately one gram per interconnect was required. This force was about three times the yield stress of the interconnect, so one would expect the interconnect to be severely distorted. This was avoided by leaving the surrounding photoresist in place after the last electroplating step.

Then all the deformation due to mating occurs in the bump of indium protruding above the resist. After mating, the structure is rinsed in acetone to remove the resist from between the two chips.

The contacts on the photodiode mesas are extremely important in affecting a proper cold weld. Gold pads will weld to clean indium and several early tests were carried out with that metal. Indium pads on the photodiodes work best. However, the indium on both the photodiode array and on the interconnects must be completely fresh. Therefore, indium is applied to the photodiode array just before mating. Storage of devices with indium pads even in a nitrogen purged box results in unsatisfactory adhesion.

The importance of timing in carrying out the various steps leading up to mating has been emphasized above. The mating procedure normally requires less than one hour.

3.6 Results of Mating Experiments with Test Chips

Mating experiments were carried out with test chips to demonstrate the feasibility fo the cold welding technique. In preliminary tests with both dummy and functional photodiode chips some requirements for successful mating were developed as follows:

1. Indium on both the interconnect and the photodiodes must be absolutely fresh as discussed in the last section.
2. The substrate material for the photodiode array must be polished flat on both sides prior to epi-layer growth.
3. The swivel block which supports the photodide array during mating must be very flat to apply uniform pressure during mating.
4. The resist surrounding the columns during mating must be smooth on the top surface. Otherwise the observed

image of the photodiode mesas will be distorted and alignment difficult.

5. The mating must be carried out under very clean conditions. A piece of lint or dirt more than two or three μm thick will prevent uniform mating.

6. The silicon chip must be constrained from flexing.

It is this last item which caused the greatest difficulty and prevented complete mating to the test chips. Because the chip was able to flex slightly when the mating force was applied, the mating bumps on the interconnects toward the edge of the array were compressed more than those in the center. Therefore, when the force was relieved, those connections on the outer edge were severed. Since the columns were surrounded by photoresist, they were unable to yield. So all the strain due to the bending of the silicon had to be accommodated in the plane of the contact to the photodiode. This condition was not relieved by improvements in the flatness of the vacuum chuck because only a small deformation was necessary to cause the observed results.

That good cold welding was achieved is demonstrated by the SEM photograph in Fig. 31. This shows the region of an interconnect which has been severed by pulling apart a mated sample. It is seen that the deformation is characteristic of plastic flow. This result illustrates the ruggedness of the hybrid structure since proper cold welding results in a structure that can be separated only by rupturing the interconnects.

Normal procedure for testing diode arrays mated to test chips was to probe the single element striplines of the test chip in a specially designed probe station that maintained the sample near 77°K. However, detector performance could not be determined in a way which simulated the required operating conditions. To do this, a

Fig. 31 Scanning electron micrograph of fractured interconnect.

mated array was mounted on a multiple pin header and wires bonded directly to the single element striplines.

One sample bonded in this way was cycled nine times from room to low temperatures. Five of those cycles were to 8°K. On several cycles the vacuum was broken and re-established. Figure 32 shows the I-V characteristics at 77°K of the 14 devices along a single diagonal that were measured. Note the vertical scale is 500 nanoamps. Zero-bias impedances at 77°K of these devices was $4x10^4$ ohms except for one which was lower as can be seen. These characteristics were unchanged from the first cycle to the last.

Noise measurements were carried out on these 14 devices at reduced temperature. The background flux for these measurements was $2.25x10^{14}$ photons/cm^2 sec. In all devices, including the more leaky one, the total measured noise was just that due to photocurrent shot noise at both 8°K and 30°K. The measured D^* in this background was $(1.74 \pm .06)x10^{12}$. These devices were not AR-coated.

In this test, devices out to 11 elements from the center were measured. The yield of connected devices in the central 16x16 region of the chip was virtually 100% with the yield decreasing toward the outer edge. Devices that were not connected resulted from flexing of the silicon chip as described before and not from a failure of the interconnect. These results indicate that the approach to the interconnect problem is correct and leads to a reliable hybrid structure. This assembly survived a great deal of handling, including a preliminary probing, mounting in a package and bonding to the striplines, in and out of the dewar a couple of times and attachment of the ground contact to the photodiode array. During all this, there was not a single contact lost.

3.7 Results of Mating Experiments with Multiplexers

Mating of the photodiode array to the multiplexers is essentially the same process as just described for the test chip.

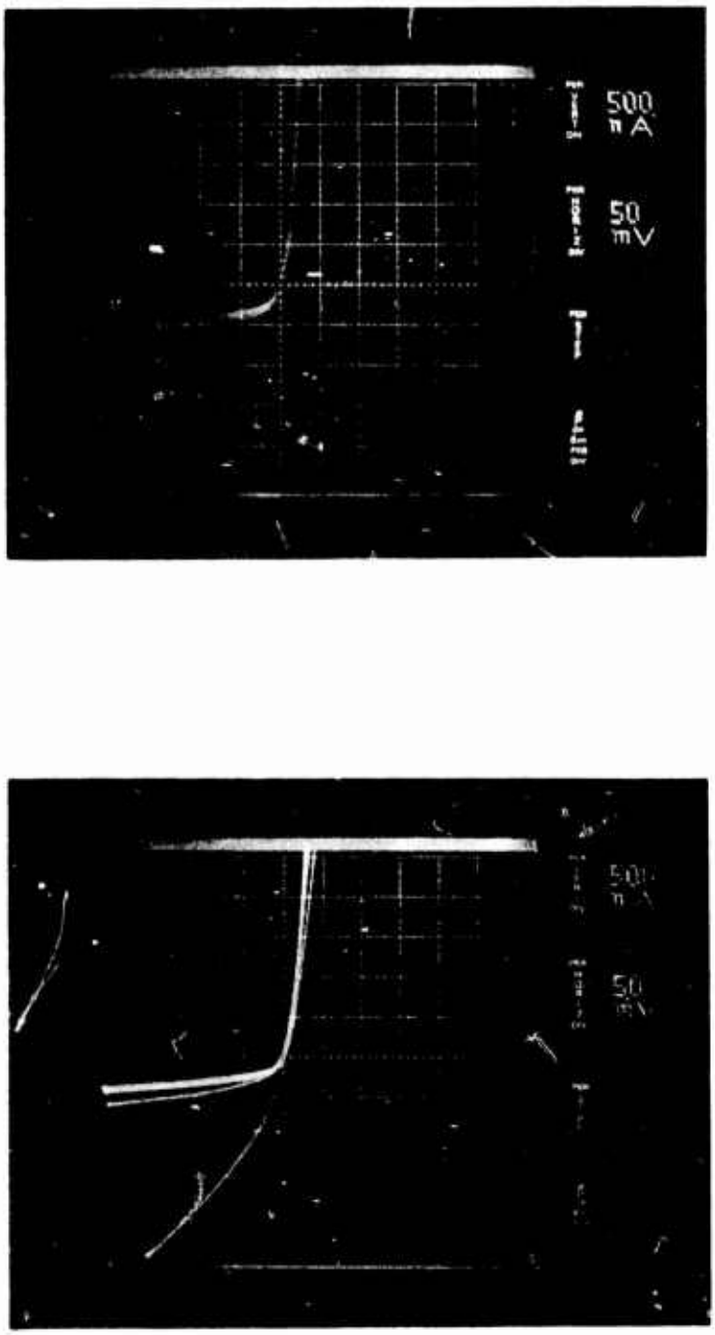


Fig. 32 Current-voltage characteristics of 14 devices of a PbSnTe array mated to a test chip.

However, the problems with bending of the silicon wafer as described before were not encountered because the small multiplexer dice were supported around all edges by epoxy. Since an antireflection coating was not applied to the multiplexer dice, observing the photodiode mesas was more difficult, but by taking a little more time, just as accurate alignment could be obtained as with the test chips.

Although most of the multiplexers purchased for this program were utilized for tests during various phases of the program or were lost due to processing problems discussed earlier, several were processed with high yields of interconnects suitable for mating. Of these, one was destroyed during bonding of wires to the multiplexer access pads and at least one failed to clock properly at low temperatures. The results to be presented below represent the best obtained during the course of the program.

The first information obtained from the mated array is the yield of interconnections between the photodiode mosaic and corresponding cells of the multiplexer. Array No. 48 exhibited a yield of interconnects of 90% after initial mating. This number was obtained by clocking the array at room temperature and monitoring the output of the video line through the recharge amplifier. With a small applied bias any connected photodiodes appear as shorts at room temperature and can be easily distinguished from the opens.

The 90% yield represents nearly complete mating of the center 30x30 array (2 elements here were missing). Most of the elements in the outer row around the array were not connected. This result was also observed on a number of mated arrays.

After close analysis of the interconnect growth process, it was determined that the way in which the photoresist built up during processing for the last interconnect growth resulted in a wider cross-

section for the outer row of interconnects. Because the deposition of metal occurred at the same rate for all the interconnect sites, those on the outer row were considerably shorter. Although there was some contact to these interconnects, the deformation of their mating bumps was not adequate to affect a proper cold weld. A procedure was implemented to correct this problem but no samples were mated with full uniform columns.

Making corrections for this known effect, the yield in a 30x30 array was essentially 100%. Since the array must be operated at 25°K, the next information to be derived was the yield of interconnects after cooling to the operating temperature and particularly after cycling between room temperature and 25°K. Figure 33 is a plot of the fraction of interconnected devices out of those possible versus the array size taking subsets of the mated 32x32 array. This data is taken after the fifth thermal cycle to 25°K. Subsequent thermal cycling showed that this yield had been essentially stabilized.

It should be pointed out that the interconnects on this array were only 40μm high. The estimated requirement for a .128" x .128" array was that the interconnects should be 50μm high. From Fig. 33 it can be seen that the yield for a 26x26 array was 99.3% so scaling the array size linearly with the column height indicates that 50μm columns would have resulted in a fully mated 32x32 array. Indeed, experiments where arrays of shorter columns were mated showed a smaller area of high yields. Unfortunately, those multiplexers which contained higher aspect ratio columns failed to clock after bonding and mounting. The causes were traced to multiplexer defects and not to processing of the interconnects.

Charge storage measurements were carried out on devices from array No. 48. Because of the tedious nature of the charge storage measurements only a small number of devices were actually studied.

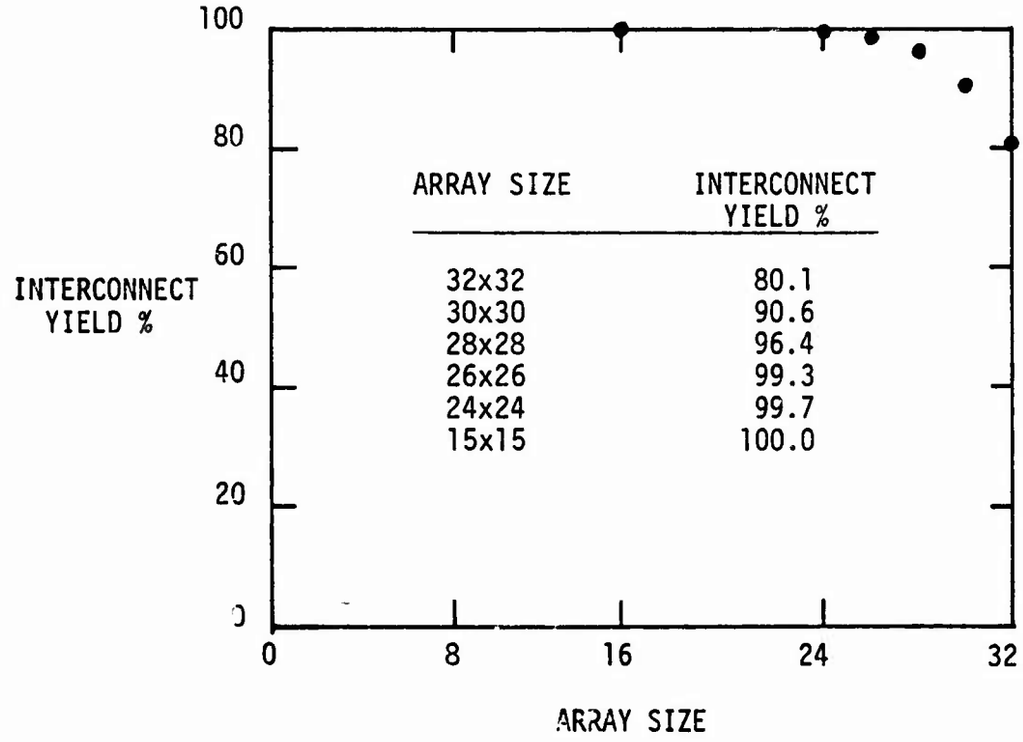


Fig. 33 Plot of number of interconnects versus size of array subset after fifth thermal cycle of hybrid structure.

The computer interface was not completed in time to carry out the automated analysis of device characteristics.

For the charge storage study, four devices were utilized. The recharge amplifier output is shown in Fig. 34. There are two pulses for each device corresponding to two different flux levels as explained below. Numbers are assigned to the devices is indicated in the figure. Devices 3 and 4 exhibited very little leakage, but devices 1 and 2 had somewhat greater leakage current as indicated by the more negative output voltage. Zero output level is indicated by the horizontal line. Two dummy diodes built into the multiplexer circuitry are seen on the far right in the figure.

For these test, the array was set up in a dewar which allowed a controlled amount of infrared radiation to impinge on the hybrid array. Using a liquid nitrogen cooled source, the number of photons incident on the detectors was negligible. With a 300°K source external to the dewar, the incident in-band photon flux was approximately 1.1×10^{12} photons/cm^2/sec corresponding to 5.5×10^7 photons/sec incident on each detector, taking the detector area to be 5×10^{-5} cm^2.

To check for charge storage operation, the recharge amplifier voltage was measured on an oscilloscope as a function of frame time for both levels of incident photon flux at each frame time. The resulting data is plotted in Fig. 35. It can be seen that devices 3 and 4 exhibit the proper dependence on frame time. That is, both the lower and upper curves corresponding to those devices are linear with frame time. The scatter in the experimental points is entirely explained by the error in reading the zero level and the signal level from the oscilloscope. Subsequent to making these measurements, a sample-and-hold circuit was implemented allowing output voltages to be read to an accuracy better than one millivolt. With a pessimistic value of 10^{-3} volts for total electronics noise, the minimum detectable number of photons for devices 3 and 4 is approximately 9×10^5.

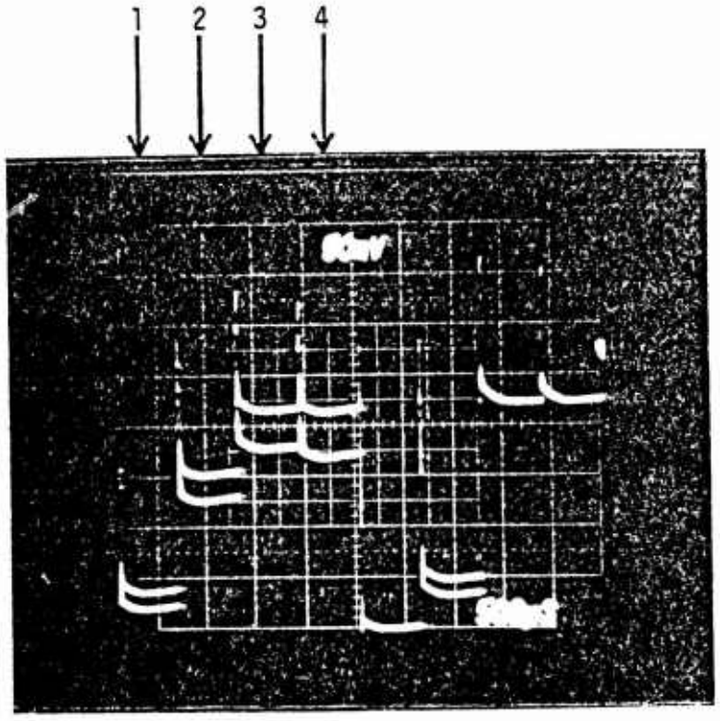


Fig. 34 Portion of the recharge amplifier output for a multiplexed array. The two levels for each pulse correspond to two different levels of photon flux.

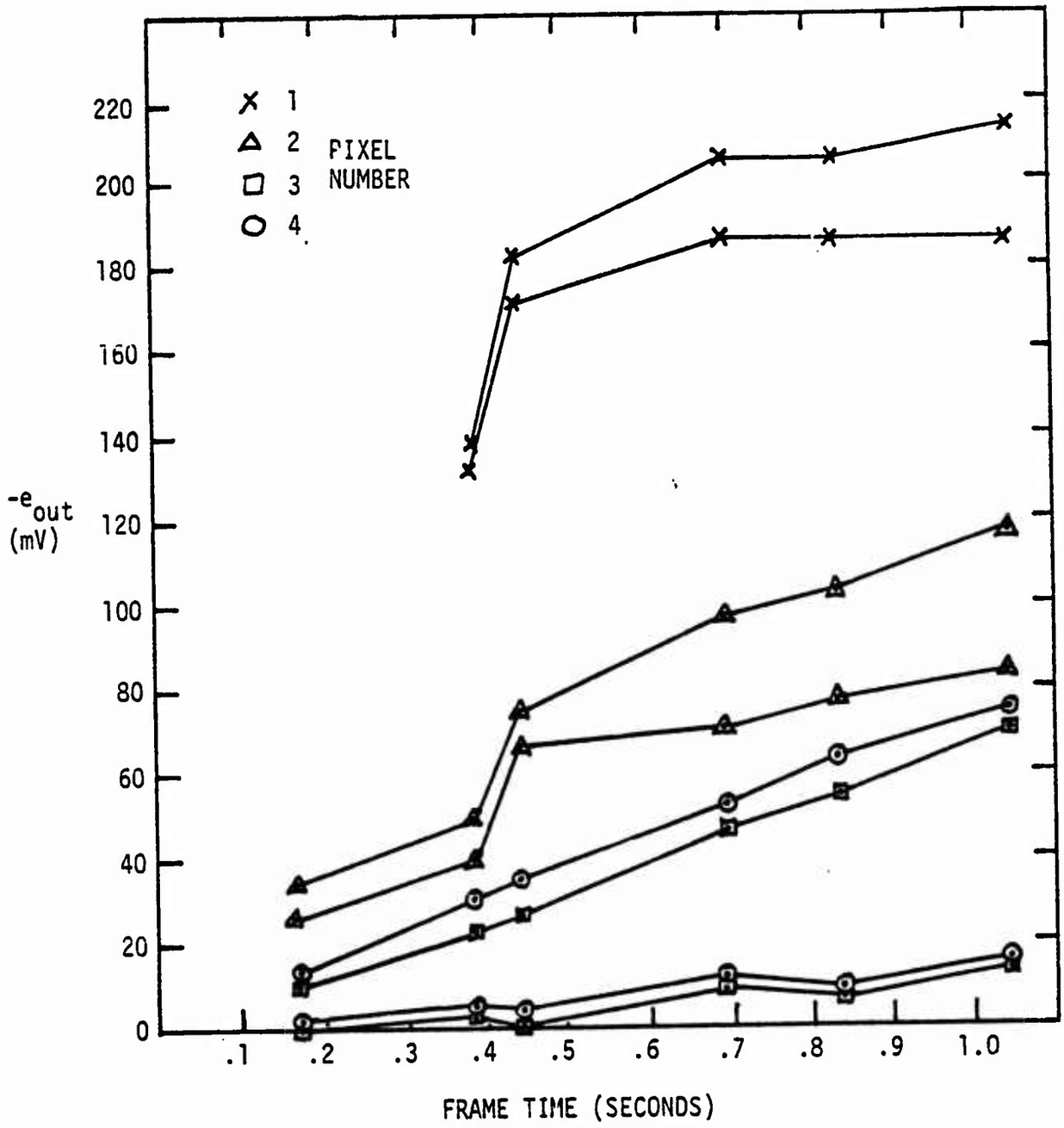


Fig. 35 Plot of recharge amplifier output voltage as a function of frame time for 4 devices from a multiplexed array.

Based on the noise characteristics of the recharge amplifier, switch array and photodiodes, we should expect minimum detectable number of photons to be at least three orders of magnitude below the value calculated above. That this was not observed in the tests described is a direct result of the dewar and recharge amplifier configuration. Since all the electronics was external to the dewar, parasitic capacitances and noise sources dominated system performance. It was found that construction of an integral cryogenic recharge amplifier and dewar system was beyond the time and funding limitations of this effort.

The curves in Fig. 35 corresponding to devices 1 and 2 show the behavior expected for leaky photodiodes. Even for no photon flux (lower curves for each device), there is a substantial recharge signal. This is because the leakage discharges the device. Device 1 shows saturation behavior, indicating that it is completely discharged by leakage beyond T_f = .45 seconds. Also the separation between the upper and lower curves is smaller because the discharged devices can store only part of the photogenerated charge.

4.0 CONCLUSIONS AND RECOMMENDATIONS

This program has conclusively demonstrated the feasibility of the direct mated hybrid structure. The following is a recapitulation of the original Work Statement with a discussion of the progress toward each of the items listed.

Task 1. Focal Plane Electronics

- "Build a MOSFET recharge amplifer."
  This part of the work statement was not carried out because a MOSFET amplifier was not necessary for this application. Instead a commercial JFET input amplifier operating at room temperature was more than adequate for the purpose of this demonstration.
- "Modify existing clock circuits to give frame times up to 3 seconds and test dynamic shift registers for this capability."
  The linear multiplexer acquired during the first phase of the program was found to be capable of at least 6 hour hold times per pixel leading to a calculated frame time for the 32x32 array of more than 6000 hours at the operating temperature. The final multiplexer was tested for pixel hold times of a few minutes, implying a frame time of many hours.
- "Test the purchased Si chips for satisfactory operation at cryogenic temperatures."
  The final multiplexers clock properly at temperatures as low as 4.2°K.

Task 2. Wafer Mating

- "Develop techniques for making indium contacts onto the silicon and PbSnTe contact pads."
  These techniques were developed as discussed in detail in the body of the report.

- "Develop techniques for mating and joining the wafers."
  These techniques were successfully implemented and utilized for the fabrication of complete operational hybrid modules.

Task 3. Test of Hybrid Array

- "Develop techniques to use minicomputer for array tests."
  Suitable techniques were designed during the course of this program but implemented under company IR&D funds after the end of this program.
- "Test the completed array."
  Tests of completed arrays were carried out to characterize interconnect yield and charge storage operation at low temperatures as described in the bulk of the report.
- "Deliver one best-effort PbSnTe-Si hybrid array."
  A complete functional hybrid module was delivered to NELC for testing.

Although major advances in focal plane technology were made during the course of this program, several aspects require further refinement. It must be borne in mind that the PbSnTe-Si hybrid structure is the most difficult structure to fabricate because of the large thermal expansion mismatch. Already since the end of this program, the techniques have proven invaluable for the mating of materials, other than PbSnTe, to the silicon FET switch arrays. If the expansion mismatch is smaller, yields of interconnects approaching 100%, even after many thermal cycles, have been achieved. In addition, the hybrid structure has recently proven its worth in the analysis of the characteristics of large photodiode arrays. The computer interface is now capable of automatically clocking to and measuring the I-V and responsivity characteristics of all detectors in an array.

While work is continuing under IR&D funds along the line developed by this contract effort, several recommendations on the future of this work can be made. These are as follows:

1. Development of a CCD multiplexer. While the FET switch array is useful for the testing of arrays and for low background applications, a more general approach is to access the devices through a CCD. This also requires the development of new types of input circuits.

2. Explore other methods of interconnect fabrication. Other possible methods of fabrication were discussed earlier in the report and some offer the potential of reduced process time and therefore increased cost-effectiveness. Also, application of the present plating techniques to growth of interconnects on entire silicon wafers prior to dicing seems straightforward at this time.

3. The use of high density interconnect technology should be useful for a variety of other types of devices. A study effort aimed at applying the techniques described in this report would be appropriate.

4. The technology base developed under this contract should be exploited in the study of infrared focal plane systems, particularly as it relates to requirements on detector and electronics performance.